K61A Training Material
Predator/Hook

. Chassis Development Overview
  - Development Background
  - Product Trend

2. Basic Training Material Block by Block
  - Deflection
  - Power

3. Block Diagram
  - System Block Diagram
  - Power Block Diagram
  - Deflection Block Diagram
  - Video Block Diagram
  - Audio Block Diagram
  - Power Block Diagram

4. Considerations Related to SVC Property and Product Defects
5. Considerations for Factory Data and SVC of SVC Mode
6. MM SLOT related information

1. Chassis Development Overview

Development Background

☐ Keen competition for Digital Ready Zone functions of CRT TVs
- Image quality improvement through digital Image processing (Pixel Plus and DRC-MF)
- Extended support of display functions for the spread of digital storage equipments

☐ Necessity of differentiation in the design of '04 Flagship models
- Change in the trend of high-end model design concept: Exterior look (Flat → Curvy)
- high-end product family look providing the Samsung' identity

☐ Popularized adoption of advanced functions to the Leader-class models
- SONY: DRC, Memory Slot and PIP function in Leader-class models (America)
- Philips: Crystal Clear and Active Control function in Leader-class models

☐ Popularized adoption of display support functions for digital storage media
- SONY: Memory Stick (Media playback, JPEC still image support for Flat 28"~36")
- Panasonic: Secure Digital (JPEG still image, and AAC sound support for Flat 24"~36" in JPN only Product Trend.

Product Trend

☐ Leading competitors are accelerating development of new digital image processing technology for improved image quality

- SONY: DRC → DRC-MF (4 times in resolution) → DRC-MF V1 → WEGA Engine
- Philips: Pixel Plus (2.7 times in resolution)
- Samsung: DNIe → DNIe 2

☐ Various sound technologies are supported

- Leader-class F100Hz models adopt the Virtual Dolby sound as a default option.
- Flagship F100Hz models adopt the Digital surround systems such as Dolby Digital, DTS, and Dolby Digital Pro Logic.

☐ Speaker specifications (of F100Hz, 32" model)

- Leader-class: 2X10W (L/R) is default. Some models are provided with 30W Sub Woofer
- Flagship: 2X20W (L/R), 1X20W (Center), 2X15W (Rear), and 1X30W (Woofer) are provided.

☐ Popularized adoption of advanced functions to the Leader-class models

- SONY: DRC, Memory Slot and PIP function in Leader-class models (America)
- Philips: Crystal Clear and Active Control function in Leader-class models

☐ Popularized adoption of display support functions for digital storage media

- SONY: Memory Stick (Media playback, JPEC still image support for Flat 28"~36")
- Panasonic: Secure Digital (JPEG still image, and AAC sound support for Flat 24"~36" in JPN only
- Product Trend.

□ Expanded connectivity for connections with peripheral equipments

- NT: For F100, connectivity specifications of Leader-class and Flagship are similar.
  * Trend: A/V input (3 Rear and 1 Front), S-Video (2 Rear and 1 Front) and Component (2)
  * Some flagship models for the US market support DVI input jacks

< Comparison on specifications with the competing models (F100Hz High-end class) >

Europe	Sony	Philips	Panasonic
Design			
Model	KV32FQ70 : 1,050 Pound	32PW9308: 979 Pound	TX32PD30C : 1,150 Pound
Main S/P	DRC-MF	Pixel Plus	Tau TV
Picture	100Hz Digital Plus Digital Noise Reduction Auto Noise Reduction Virtual Picture Stabilizer	100 Hz Digital Scan Digital Natural Motion Digital Crystal Clear Widescreen plus	8x Density Picture- GIGA P/scan, 100Hz Super Digital Scan 3D Picture Noise Reduction, Twin Digital Comb Filter
Sound (RMS)	Virtual Dolby BEE 3D Sound 2 * 10W, 15W Subwoofer	Dolby Virtual 5 On board Speakers Built-in Center & Sub-Woofer Speaker	virtual Dolby 2 * 20W, 24W Subwoofer L/R Tweeters Direct Fixing Speakers
Function	Memory Stick Slot Fastext + 2000 Page memory PIP : 1 Tuner	T100 Preset Channels Easy Text: 1200 Page Level 2.5	PIP : 1 Tuner Color Balance Adjustment QLINK
Interface	3 SCART RGB on 1&2 Scarts	3 SCART 2 Side-AV(S-Video, RGB, H/P)	4 Scart DVD Progressive Scan Input

2. Basic Training Material Block by Block

Deflection

Basic Architecture of a CRT

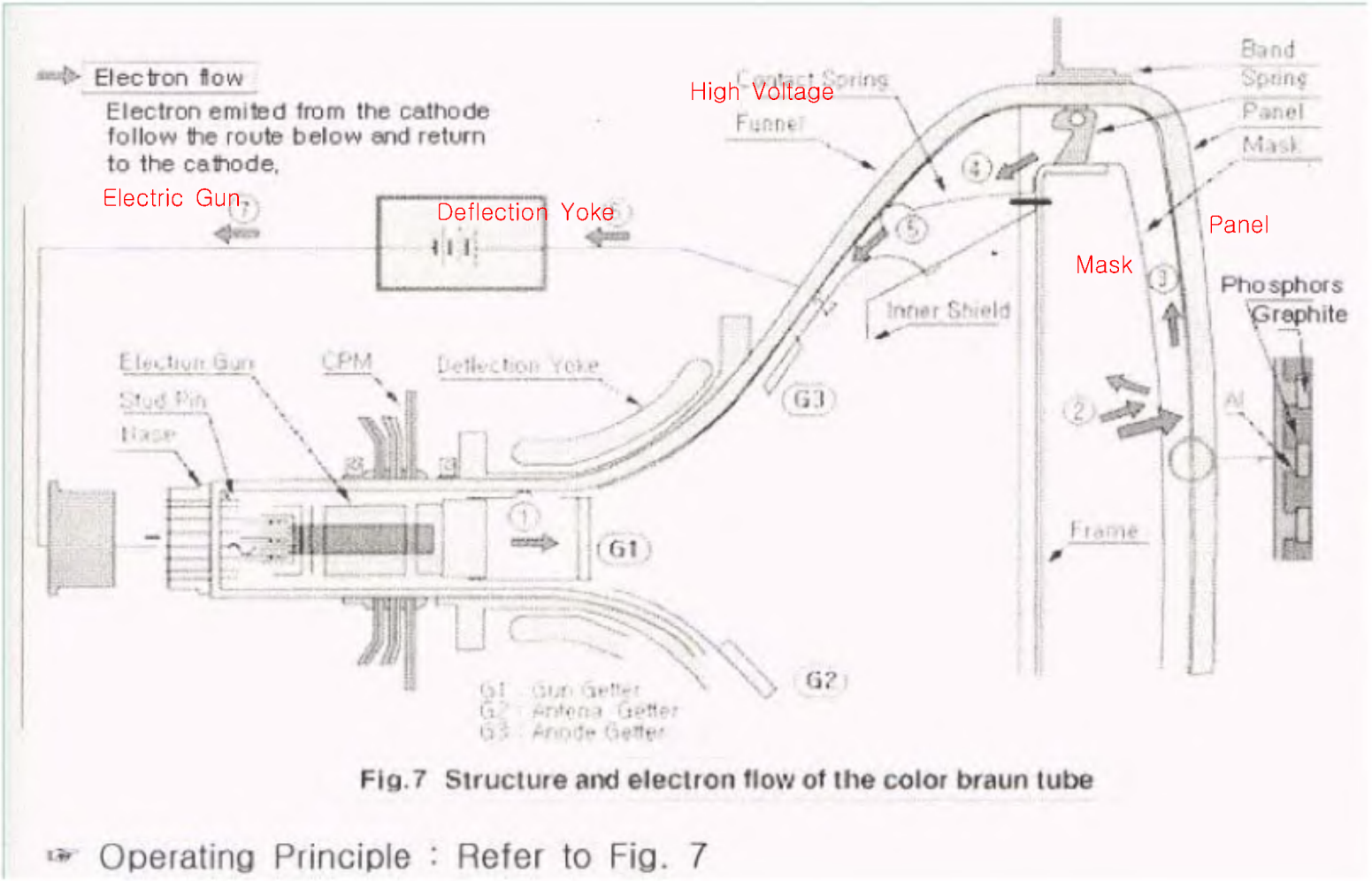
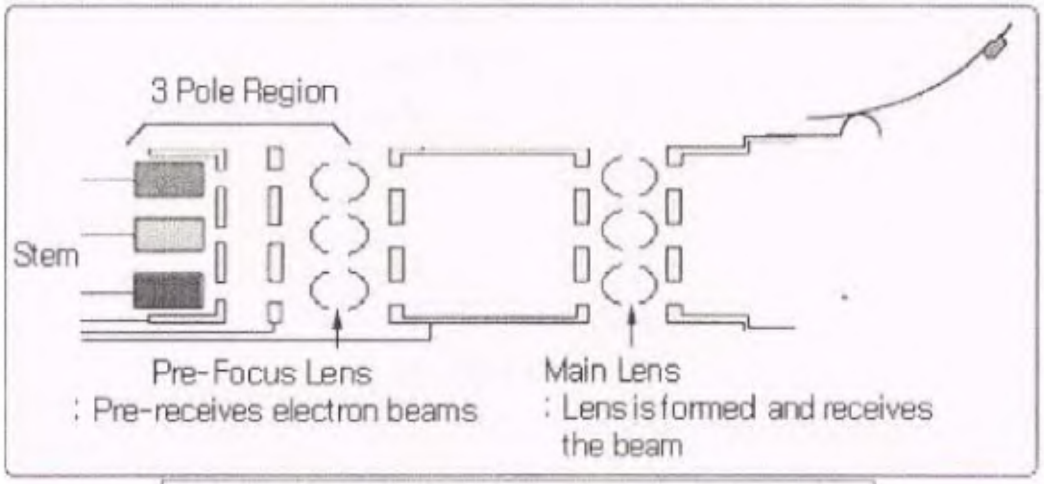


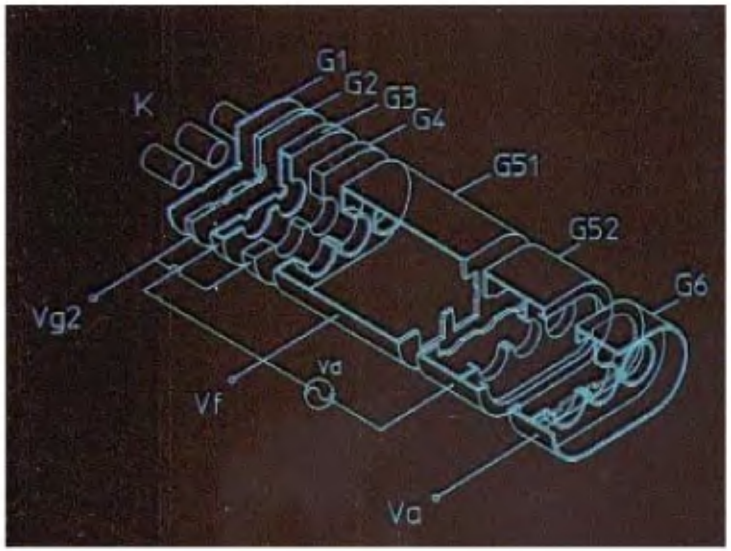
Fig.7 Structure and electron flow of the color braun tube

☞ Operating Principle : Refer to Fig. 7

Basic Architecture of an Electron Gun



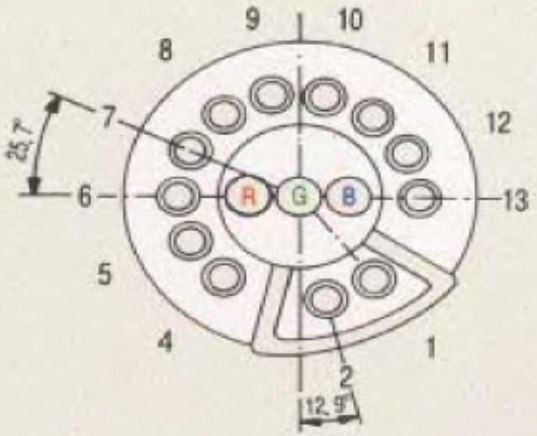
(a) An example for the structure of the electron gun



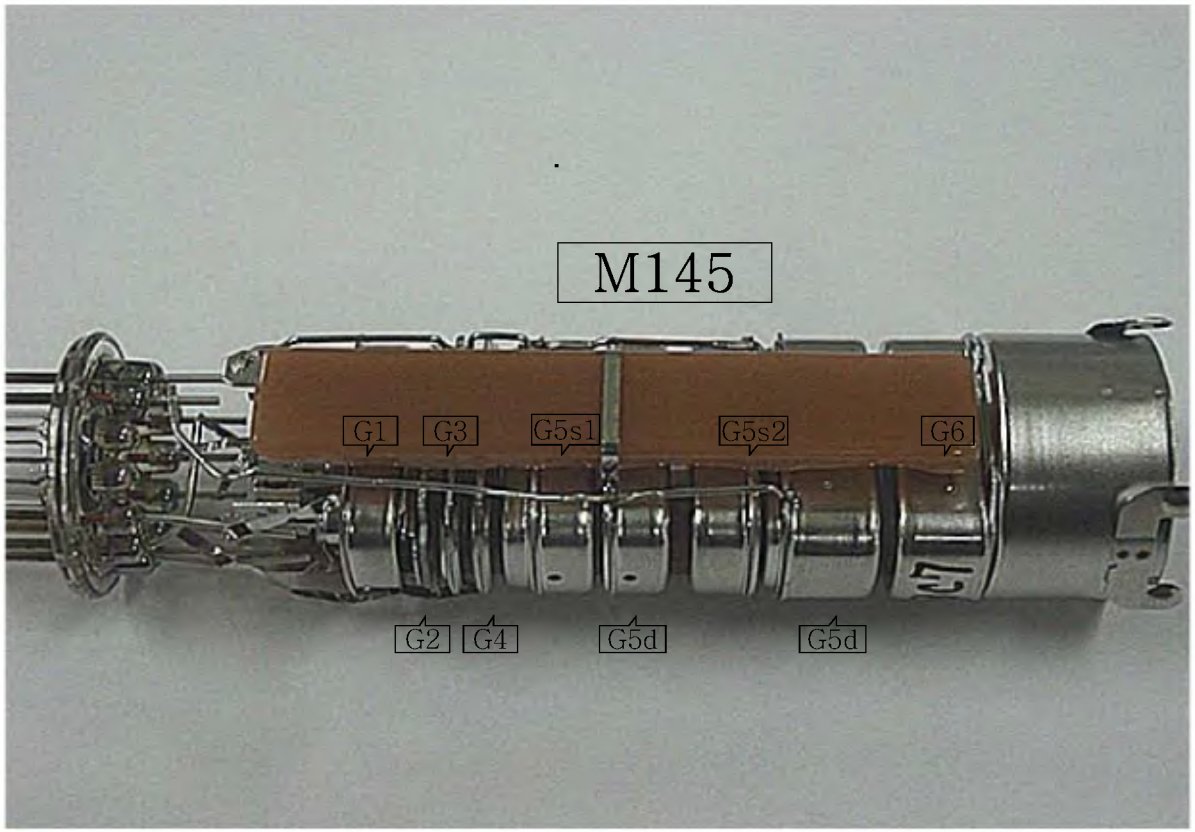
Base designation : EIA B10 - 301

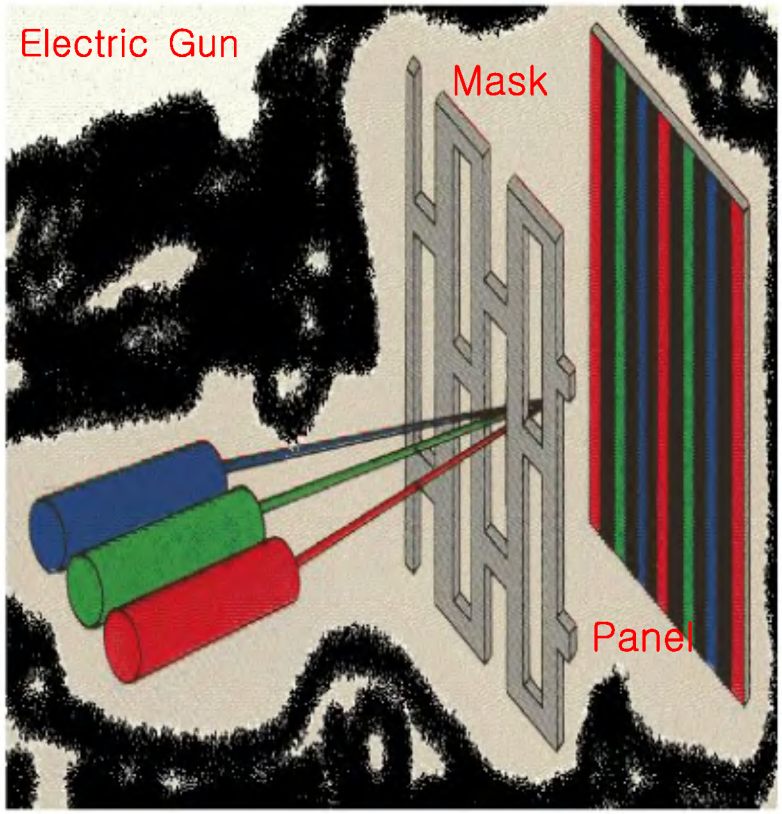
Pin No. Electrode

1 Grid No. 3 & No. 5 - B(Static)
2 Grid No. 5 - A & No. 5 - C(Dynamic)
5 Grid No. 1
6 Cathode of Green Beam
7 Grid No. 2 & No. 4
8 Cathode of Red Beam
9 Heater
10 Heater
11 Cathode of Blue Beam
12 No connection (Reserved)



Color Display Mechanism by the Architecture and Mask of an Electron Gun





Basic Operations of Signal Deflection

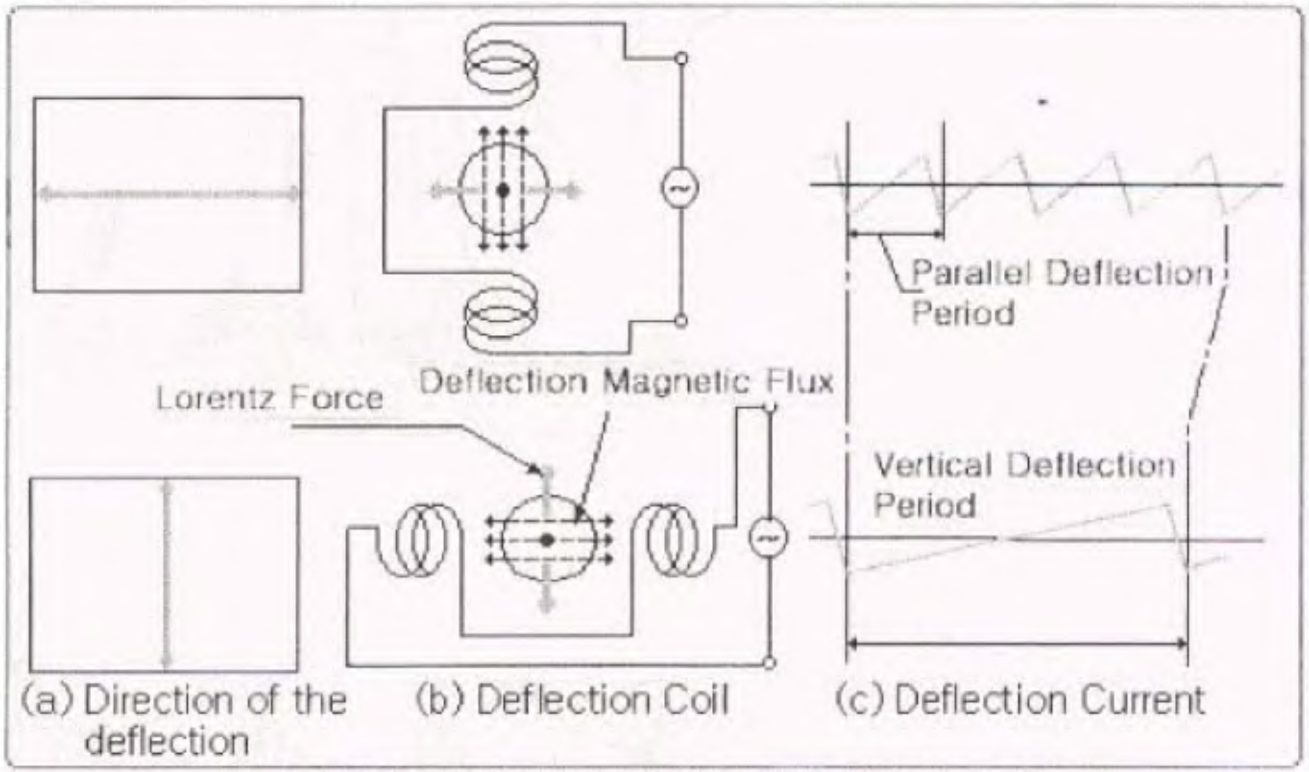
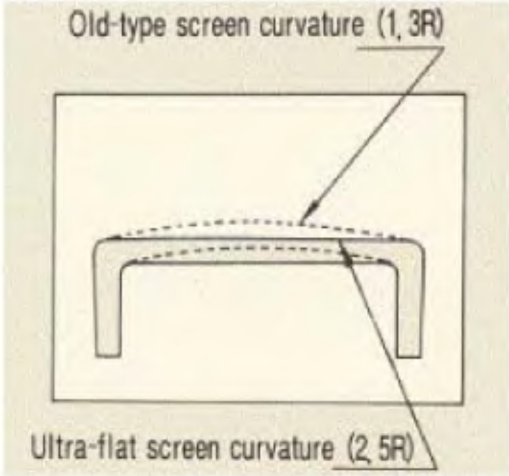
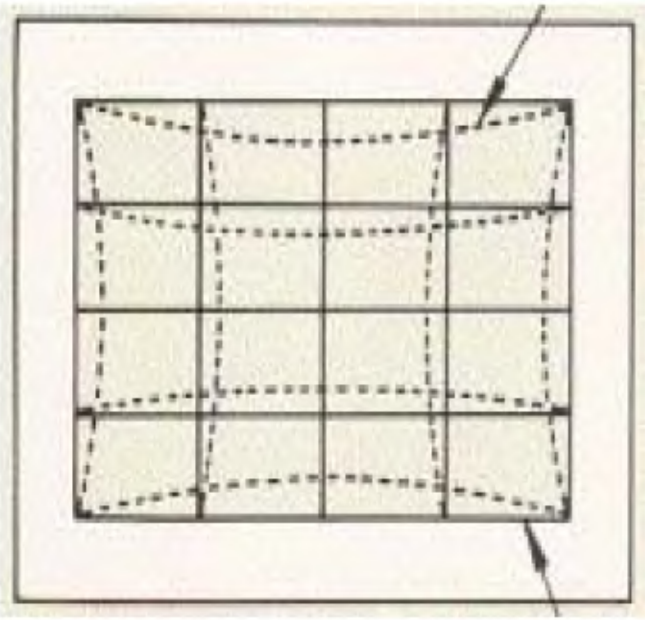


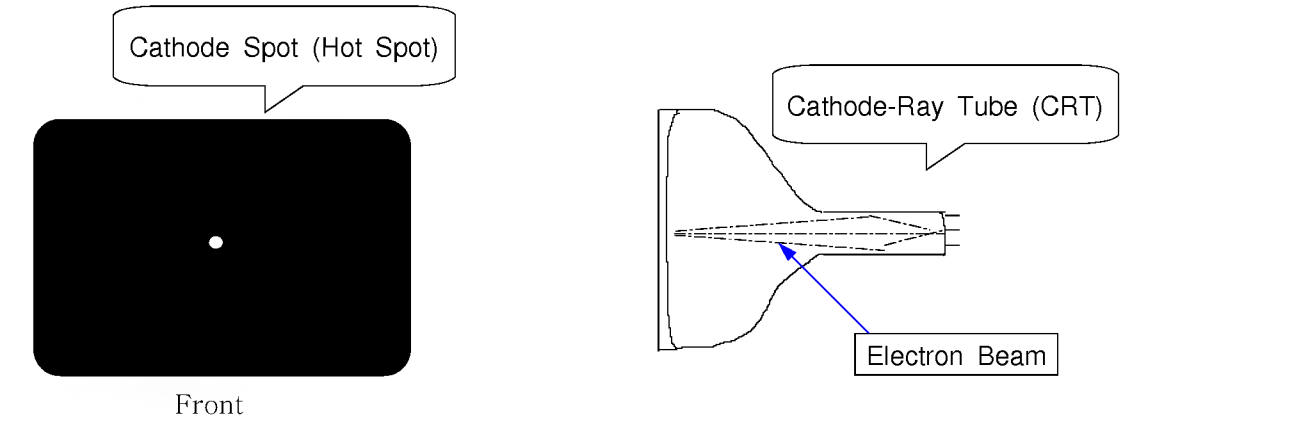
Fig. 10 The principle of the deflection coil



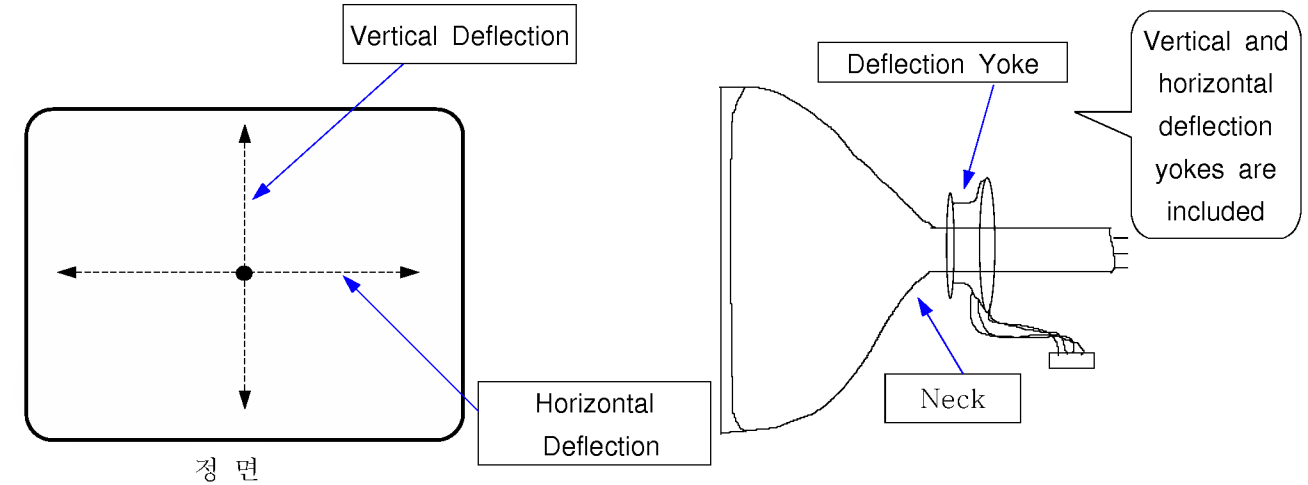


Deflection

- **Deflection**: The electrons that are emitted from the electron gun draw a straight line towards the screen, accelerated by high voltage, and therefore, if there is no other force it will only make the phosphor in the center to emit. Video signal supplied to the electron gun determines the brightness of the phosphor according to the signal. Still it makes no moving image but the moving (changing) the beam in the direction of left, right, up and down in the order of scanning should draw a video. Cathode spot can be moved by the magnetic force. The part that is attached to the funnel cone region and acts as a deflector is called the Deflection Yoke. The magnetic flux for deflection of horizontal injection is horizontal Deflection, and the magnetic flux for vertical deflection is Vertical Deflection Magnetic Flux.

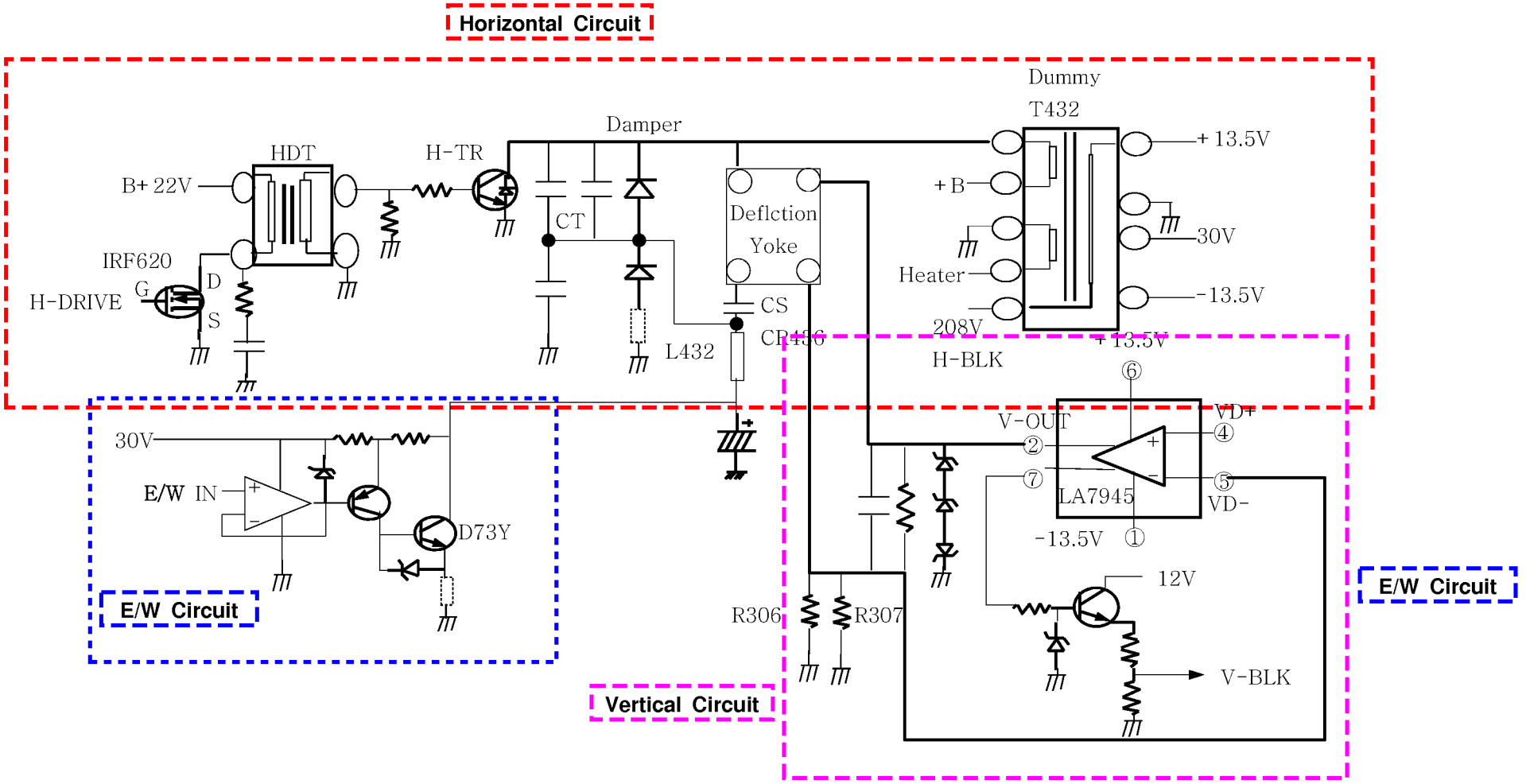


Without deflection, only the phosphor in the center emits light

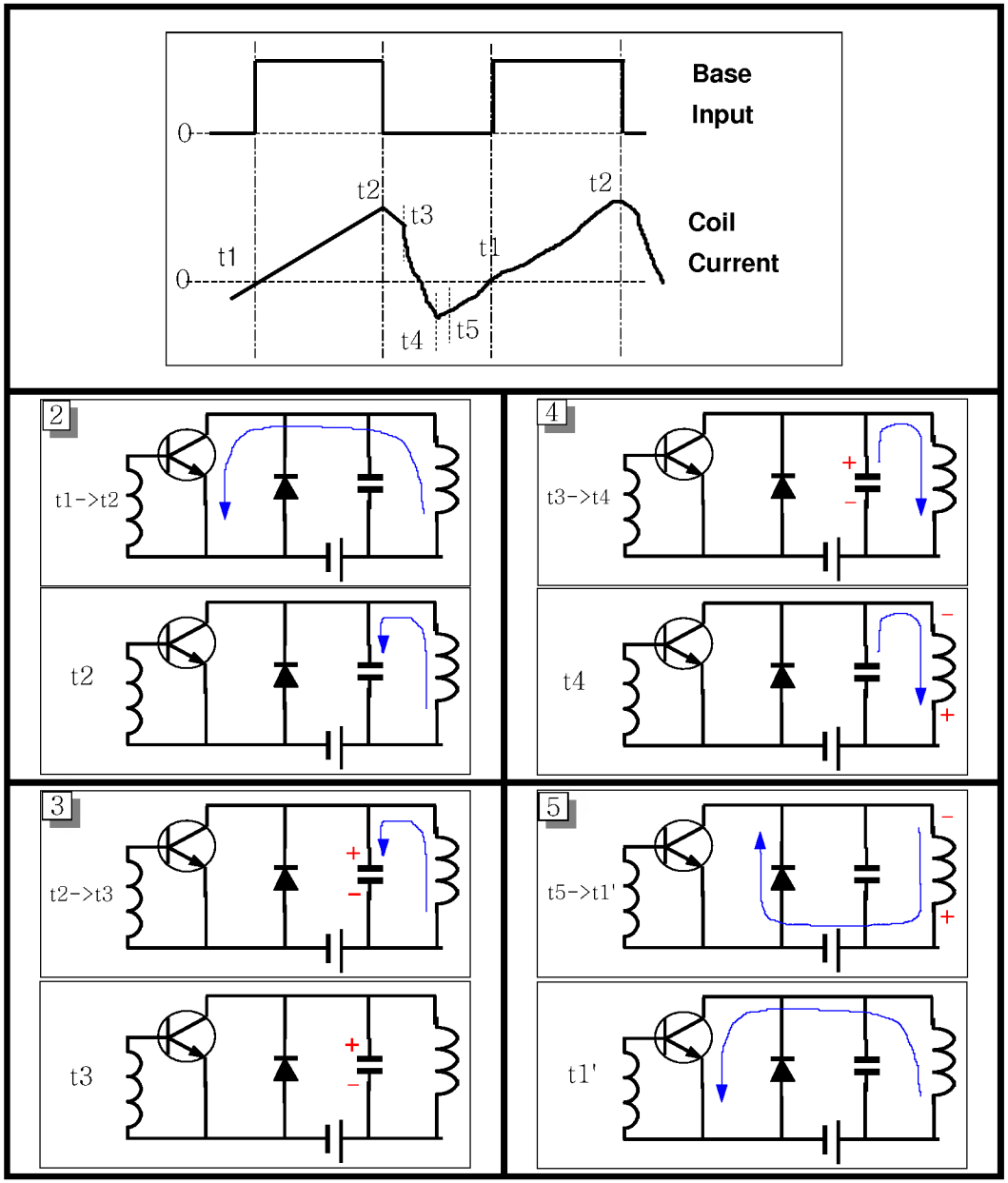


By using deflection yoke, electron beam is moved up or down, left or right

■ Deflection [Vertical/Horizontal] Block Circuit Diagram



■ Horizontal Basic Operation



① When the Tr is off, no current flows through the diode because reverse bias is applied to the diode. (before t1)

② If positive voltage is supplied to the base, the Tr is activated, and linearly increasing collector current flows through the deflection coil.
* The smaller inductance of the coil or the higher voltage of the power source raises the current. (t1->t2)

③ If the base input voltage is turned into negative pulse, the Tr is changed to cut-off and the collector current reaches 0. However, coil current flows charging the resonance capacitor, and the current drops down to 0. Since it begins (t2->t3), the direction of the current in the deflection yoke is reversed. (t3->t4)

④ After that, since resonance capacitor starts discharging, current in the deflection yoke is reversed. (t3->t4)

⑤ In resonance circuit of LC, the deflection yoke current charges the resonance capacitor in the reversed polarity of ③. However, since a damper diode is connected, the voltage between the deflection yoke ports forward biases the diode, and the deflection yoke current does not flow through the resonance capacitor and charges the power absorbing the resonance effect by flowing to the diode. (t5->t1')

⑥ When the current of diode is decreased to 0, the positive voltage is applied to the base of the Tr, and the Tr is restored to its original state

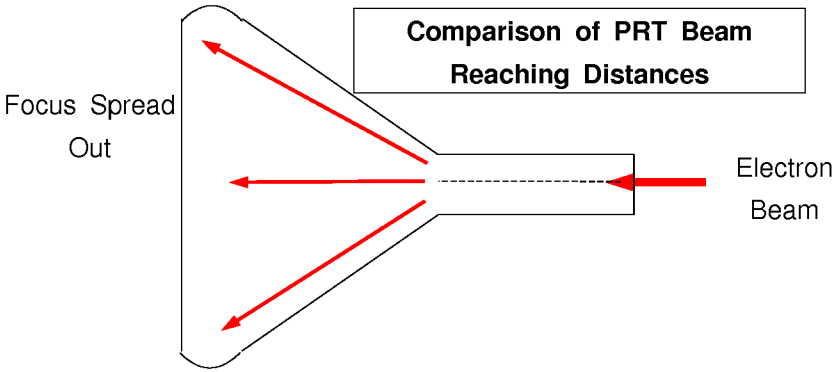
By repeating the steps to step ⑥, saw-tooth waveform current always flows through the deflection yoke. Once Tr is changed to cut-off state, positive voltage greater than that of power source is generated in the deflection yoke.

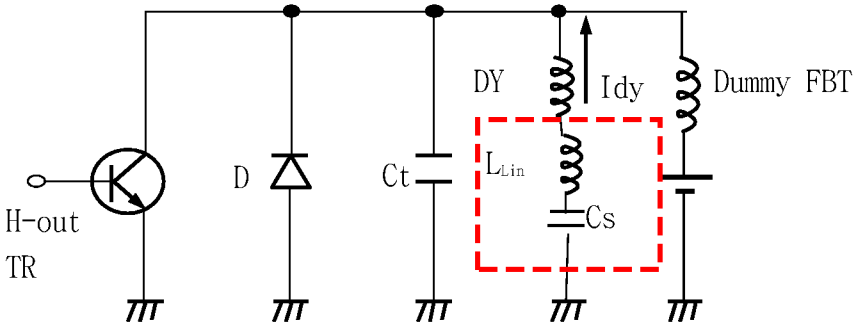
* Supplying 15.734kHz pulse to the base-emitter junction of the transistor provides periodic saw-tooth waveform current to the deflection yoke by the switching effect of the transistor

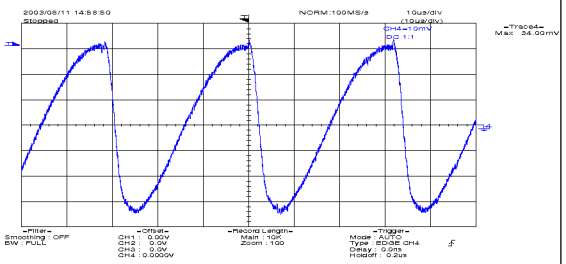
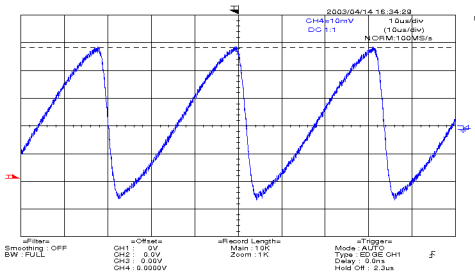
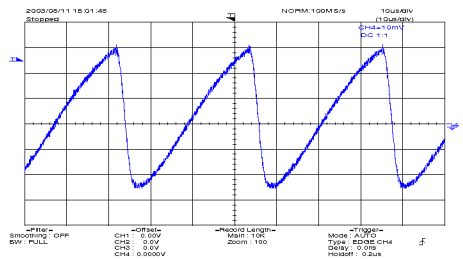
■ S-CORRECTION:

S-CORRECTION: Since the front part of the PRT is not sphere, but flat, reaching the phosphor plane is not even The beam spreads because the distance from the gun to the corner is longer than the distance to the middle to have sparse appearance on the corners. CS capacitor and Linearity coil are used to adjust the deflection current to S shape so as to control the sharpness of the beam.

※ When the capacity of CS capacitor is high, the deflection current maintains straightness because the effect of the capacitor is negligible. The less capacity of the capacitor, the more S-shaped is the deflection current.

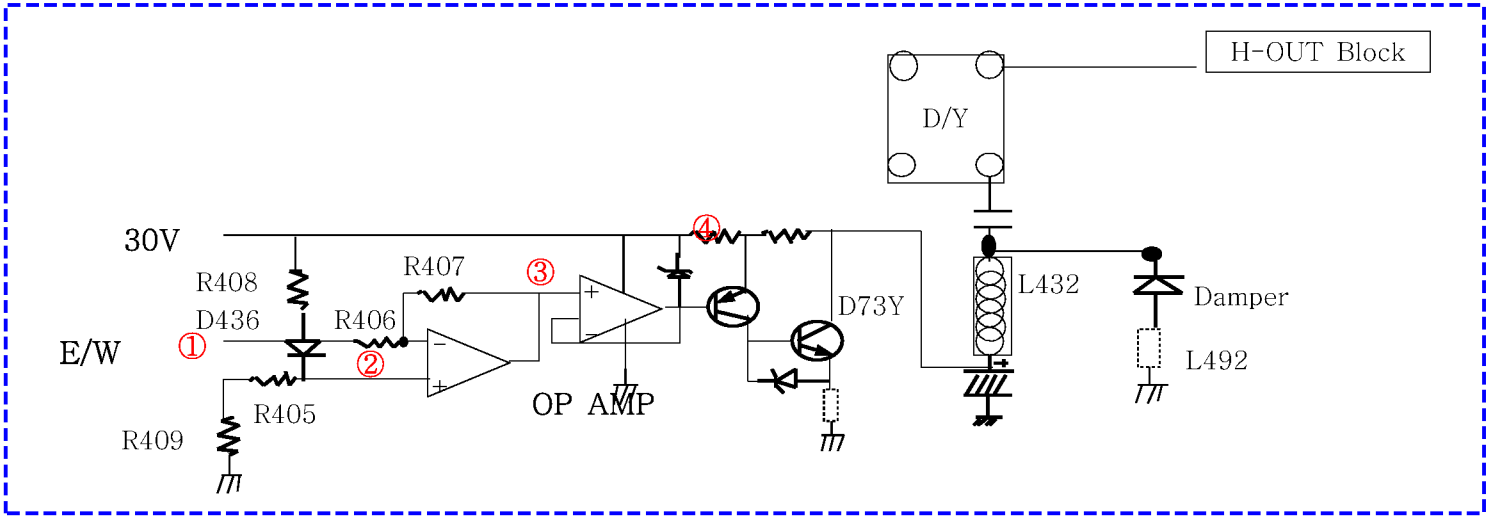


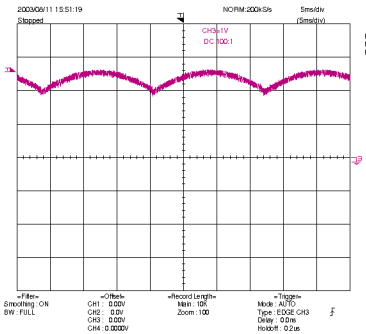
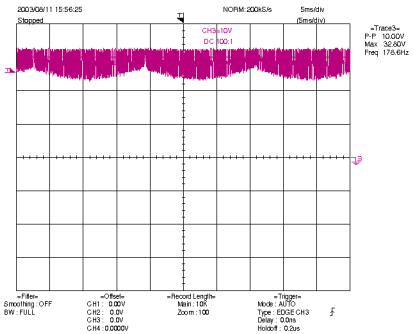
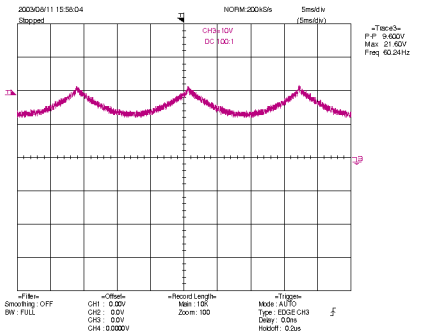
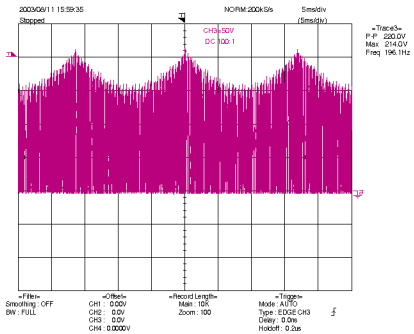


CS Capacitor[274]=> Horizontal Screen Enlargement	CS Capacitor[564]=> Normal Screen	CS Capacitor[105]=> Horizontal Screen Reduction
		

■ E/W Circuit Operation

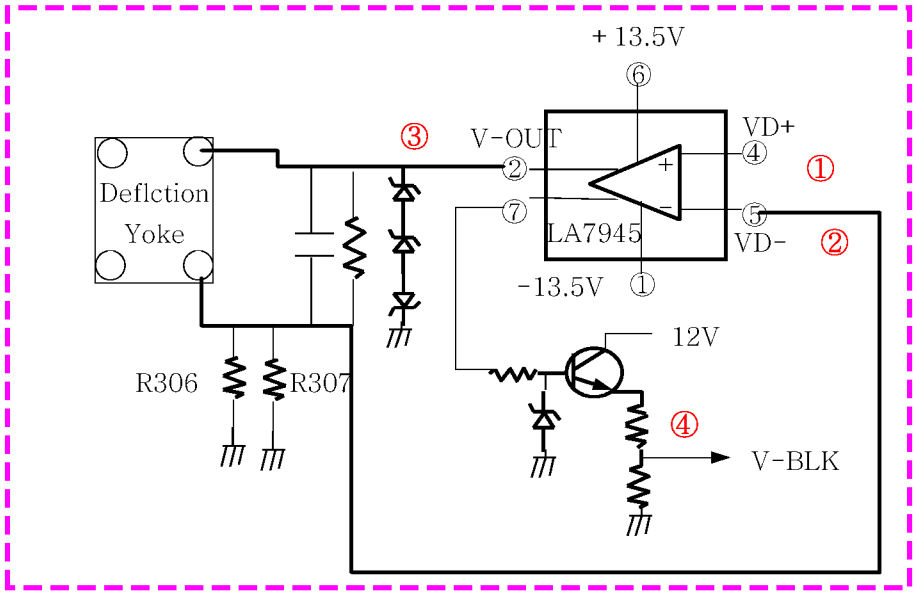
E/W Circuit Operation: This circuit is horizontal margin guarantee, and horizontal correction circuit. Due to the limitation of horizontal deflection capability, Cg adjustment grows when there is no E/W circuit. To compensate this problem, E/W waveform is supplied to pin 1 and returned through pin 2 in the main deflection IC. Using d-73Y, and amplifier L432 [WIDTH COIL], horizontal beam is corrected.

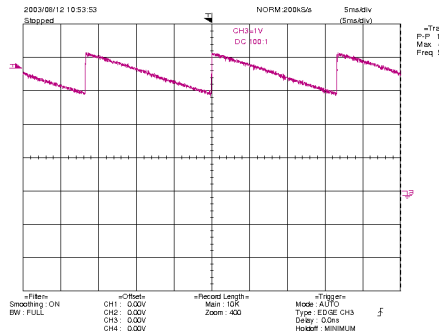
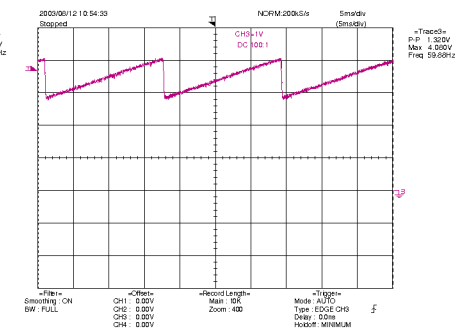
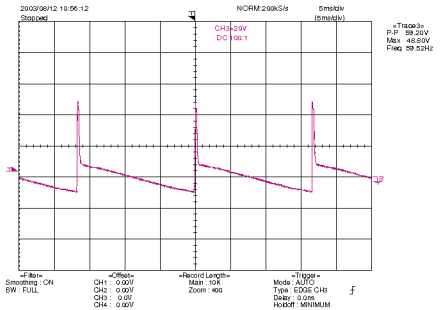
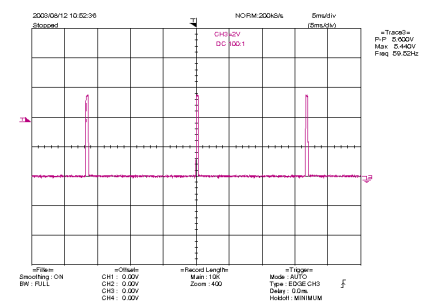


①E/W Input	②OP AMP Output	③D-73Y Output	④L432 Waveform
			
Average Status MAX:2.6V ,FV:60HZ	MAX:32.8V	MAX:21V	MAX:214V

■ Vertical Circuit Operation

■ **Vertical Circuit Operation:** VD±[vertical frequency Up/Down] signals are separated and input to the vertical IC by the main deflection IC. The waveform is sent to DY through the vertical IC controls the vertical screen display.



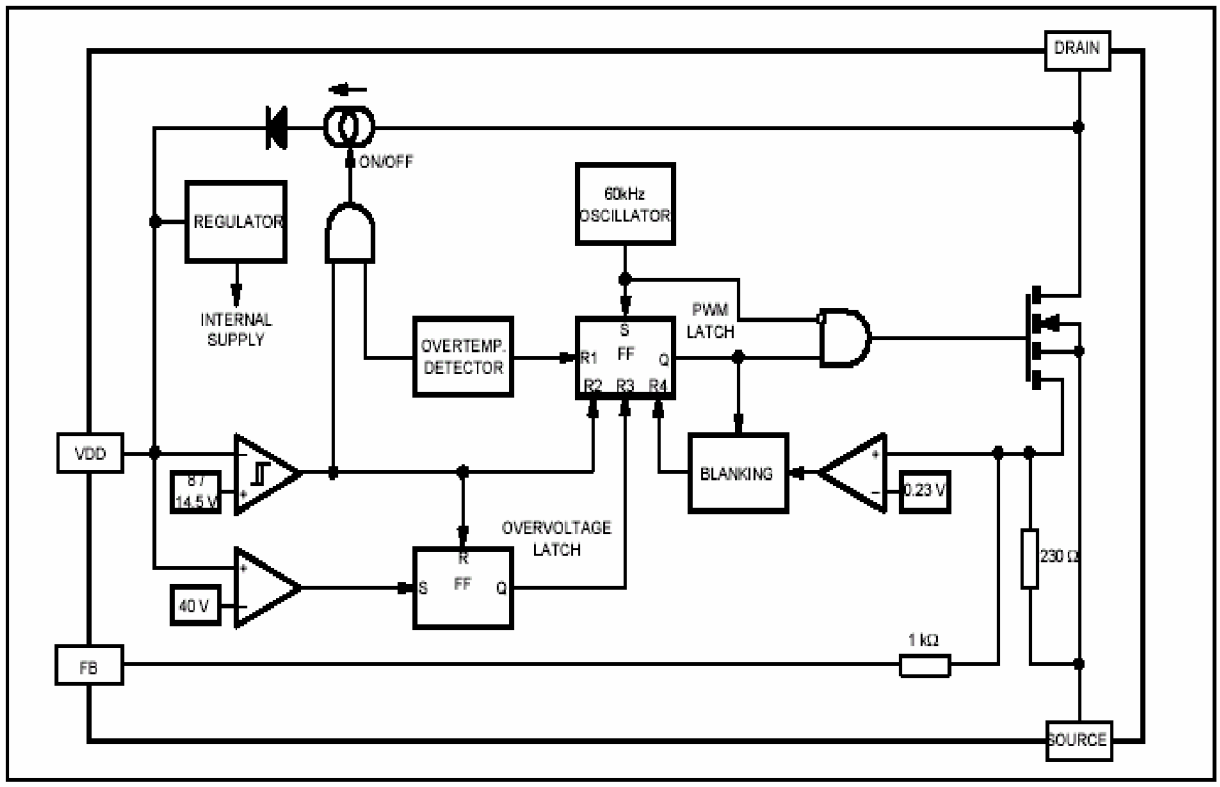
①VD+	②VD-
	
Average Status VP-P:1.28V,MAX:4.12V	VP-P:1.32V,MAX:4.08V
③V-OUT	**④V-BLK**
	
VP-P:59.2V	VP-P:5.6V

POWER

1.Stand-by IC (Auxiliary Power Supply Unit)

Viper 12A

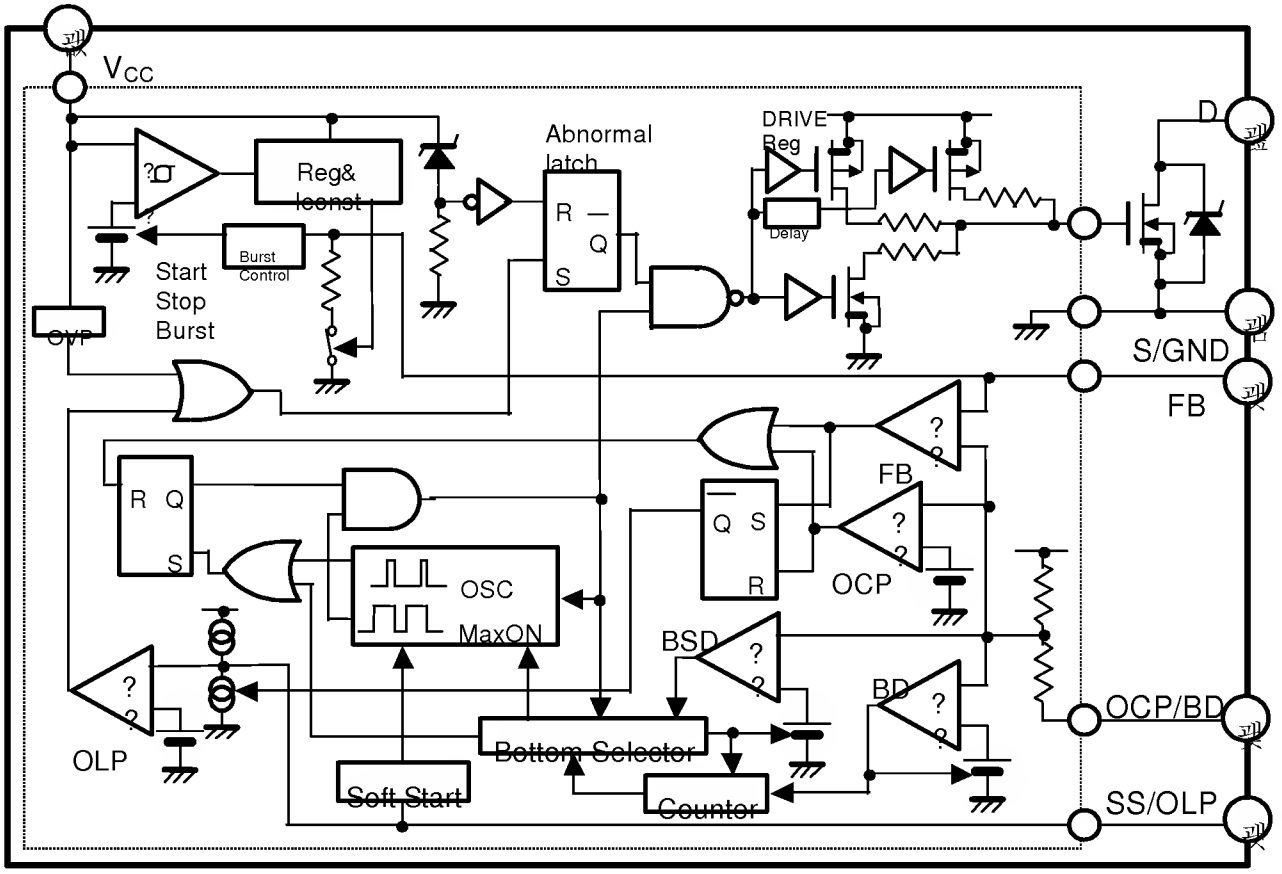
BLOCK DIAGRAM



Pin Function

Name	Functions
VDD	Supplies power to the Control Circuits. Performs the current division on High-voltage current source connected to the Drain. A hysteresis comparator monitors the VDD voltage (Provides two separated threshold currents) VDDon: Voltage value at which the device starts switching and turns off the startup current source (typically 14.5V). VDDoff: Voltage value at which the device stops switching and turns on the startup current source (typically 8V).
SOURCE	MOSFET Power Source and circuit ground (GND) reference.
DRAIN	MOSFET Power drain. Used by the internal high-voltage current source during the startup phase, for charging the external VDD capacitor
FB	Feedback input. The valid voltage range extends from 0 V to 1V. Defined by the Peak MOSFET current.

1.Block Diagram



2. Functions of Each Terminal

Terminal No.	Symbol		Name	Functions
	STR-W6700	STR-X6700		
1	Drain		Drain	MOSFET Drain
2	-	Source	Source/GND	Source/GND
3	S/GND	GND		
4	Vcc		Power supply terminal	Control circuit power input
5	SS/OLP		Sets up a delay for overloads Soft-start setup terminal	Overload detection and soft-start Setting of the operating time
6	F/Back		Feedback terminal	Constant voltage control signal input Intermittent oscillation control
7	OCP/BD		Overcurrent protection input Bottom monitoring terminal	Overcurrent protection input Bottom monitoring terminal

2. Main Power Supply Unit (Primary Power Supply Unit)

1. Descriptions of Functions

1.1 VCC Terminal (Terminal No. 4)

1.1.1 Startup Circuit

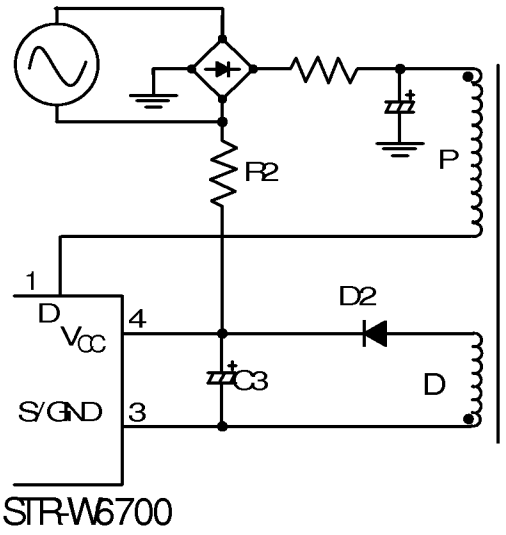
The startup circuit monitors the voltage of the Vcc (terminal No. 4) and engages the break down and the shutdown of the control IC.

The Power Source of the Control IC (Vcc terminal input) employs circuits shown in Figure 1.

At startup, the startup resistor R2 charges C3.

Set the value of R2 at higher than the holding current of the latch circuit (140μAMAX), when the AC input voltage reaches its minimum value.

If the value of R2 is set too high, the amount of the charging current used to charge C3 after the AC input will be reduced. This will cause a delay in reaching the break-down voltage. Therefore, consider the capacity of C3 at the same time.



?1 땃벍돇뿗

The voltage of the Vcc terminal decreases after the break down of the control circuit, but the decline slows down if you increase the capacity of C3. Even if the voltage of the auxiliary coil rises slowly, the Vcc terminal voltage will operate without reaching the shutdown voltage.

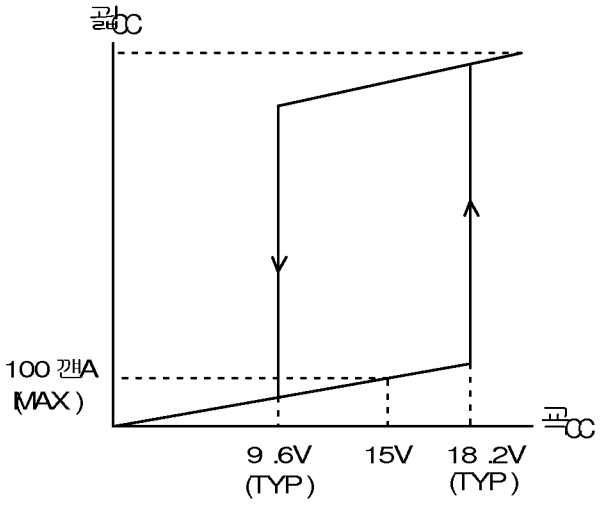
But if capacity of C3 is too high, charging the C3 after the AC input applied takes more time, causing a delay in reaching the break-down voltage.

Set the value of C3 at 10□47μF, and R2 at 47kΩ□50kΩ (for 100V) and 82K□330kΩ (for 200V) for general specifications.

As shown in Figure 2, until the control circuit starts operation, the circuit current is maintained at 100μAMAX(VCC=15 V, Ta=25℃), and R2 is allowed for high resistance.

The control circuit is triggered by the operation of the start circuit, and the consumption of current increases.

If the Vcc terminal voltage decreases below the shutdown voltage 9.7V(TYP), this device stops the control operation by engaging the Under Voltage Lockout (UVLO), and goes back to the status before starting.

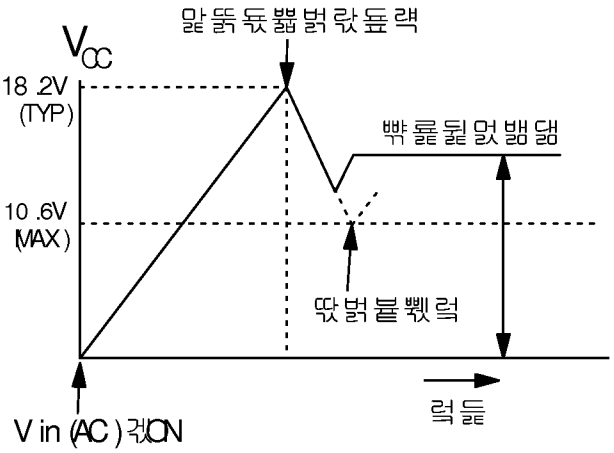


?괠 Vcc ?랜 밺댊 ?돇 뿗 밺 뿬 괠CC

1.1.2 Setup of Auxiliary Coil

After the control circuit starts operating, this device generates power by rectifying and smoothing the coil voltage of the auxiliary coil D.

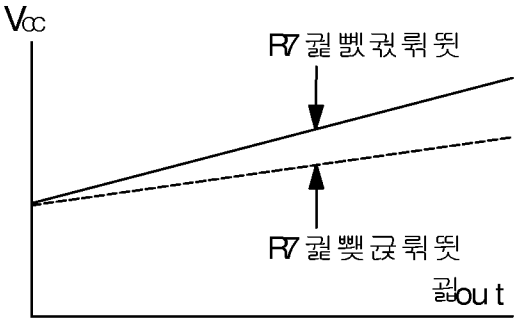
An example of VCC voltage waveform is shown in Figure 3. Since the auxiliary coil voltage does not increase directly up to the preset voltage after the control circuit starts operating, the VCC voltage begins to decrease. But the control circuit continues operating while the voltage decreases, due to the shutdown voltage is set at 10.6V(MAX).



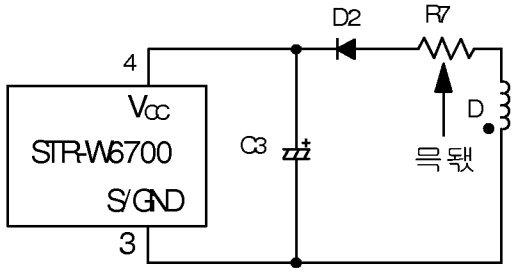
?괩 딳벍럌곡CC ?랟밺댊봥 ?쀡

The auxiliary coil D must be adjusted so that the voltage of both ends of the C3 exceed the shutdown voltage [VCC(OFF) 10.6V(MAX)] but to be lower than the OVP operating voltage VCC(OVP) 25.5 V(MIN)] during normal operations.

The VCC terminal voltage of power supply circuits may vary depending on the value of the output current on the secondary side as shown in Figure 4. It is due to the circuit current of STR-W6700 is low, and C3 is charged to a peak point due to the surge voltage generated when MOSFET is turned off. To prevent this occurrence, it is effective to add a rectifier diode and resistor R7 (1 □several tens of Ω) in serial as shown in Figure 5. The optimum value of the resistance must be adjusted in compliance to the transformer because the change rate of the VCC terminal voltage, which corresponds to the output voltage, varies depending on the structure of the transformer. Note the location of the auxiliary coil D when designing a transformer, because the change rate of the VCC terminal voltage, which corresponds to the output voltage, degrades if the primary and the secondary combination of the transformer or the combination between the auxiliary coil D and the stabilization output coil (a circuit winding used to control constant voltage) is poor.



?괪 뢜뿱밺뿬 Iout-VCC ?랟밺댊



?괫 뢜뿱밺뿬 Iout 궻뎓떫귩롤궚궸궘궋 빢룙밺뙰됷쁇

1.1.3 Over Voltage Protection

If the voltage applied between GND terminal and VCC Terminal exceeds 27.7V(Typ), the OVP circuit in the control IC operates to enter the latch mode and the control IC stops oscillation.

The VCC terminal of the power-down mode is provided by the auxiliary winding of the trans, and this voltage is proportional to the output voltage. Therefore, it operates even when the over voltage on the secondary side is output, for instance, when the voltage monitoring circuit is open. If this occurs, the output voltage on the secondary side during the over voltage protection can be expressed by the following equation.

$$\text{Vout}(\ _{OVP}\ ) \simeq \frac{\text{통상동작시}\quad \text{출력전압}\quad V_{OUT}}{\text{통상동작시}\quad \text{Vcc}} X\ 27.7V\ (TYP\ ) \qquad \text{(1)식}$$

1.1.4 Latch Circuit

The Latch circuit maintains the Low output of the oscillator when the Over Voltage Protection (OVP) or the Overload Protection (OLP) is activated to stop the Power Supply.

The holding current of the latch circuit is 140μAMAX(Ta=25℃) when the shutdown voltage of Vcc is -0.3V. Internal timer circuit of the control IC provides delay time to avoid accidental activation of the latch circuit by noise. OVP or OLP activation continues for a certain period of time activates Latch circuit.

Even if the latch circuit operates, the constant voltage of the control IC continues operating, and the VCC terminal voltage decreases because the circuit current remains high. If the VCC terminal voltage is below the shutdown voltage 9.7 V(TYP), the circuit current falls below 140μA(Ta=25℃) and the VCC terminal voltage starts to increase.

When it reaches the break-down voltage 18.2 V(TYP), the circuit current starts to increase again, lowering the VCC terminal voltage. During the operation of the latch circuit, therefore, the VCC terminal voltage moves between 9.7V(TYP) and 18.2V(TYP), preventing the VCC terminal voltage to increase too high. Figure 6 shows the waveform example of the VCC terminal voltage when the latch circuit is activated. The latch circuit is deactivated when the VCC terminal voltage is reduced below 7.2V(TYP). Generally, cutting the AC input power shortly to resume the Latch circuit.

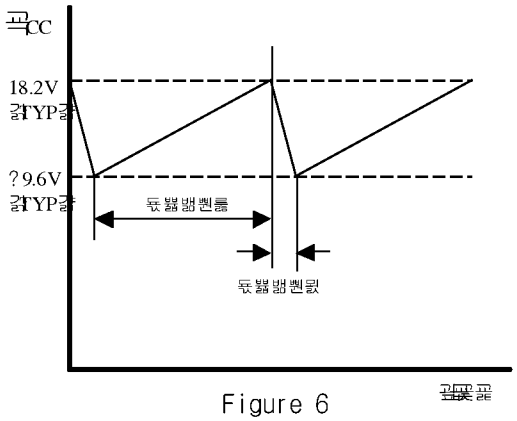


Figure 6

8.2 SS/OLP Terminal (Terminal No. 5)

The operation of the SS/OLP terminal is divided into the soft start operation and the overload protection operation during startup.

Usually, the SS/OLP terminal is connected to the condenser of 0.47μF~3.3μF.

1.2.1 Soft Start during Startup

At startup, this device charges the external condenser to the threshold voltage (VSSOLP(SS)) of the soft start by using the soft start charging current (ISSOLP(SS)) from the SS/OLP terminal. Soft start at the startup is activated by using the SS/OLP terminal voltage that changes from 0V to 1.2V at this stage.

Figure 7 shows the timing chart during the soft start.
Soft start of gradual expansion of ON width is performed by comparing the SS/OLP terminal voltage with the oscillation waveform of the control unit.
The magnetostriction noise from the transformer is reduced due to the Soft start from the Burst Standby mode increases the Drain's current gradually.

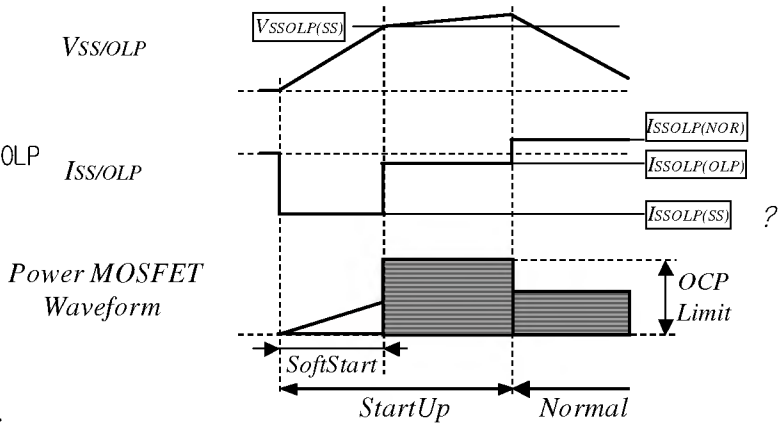
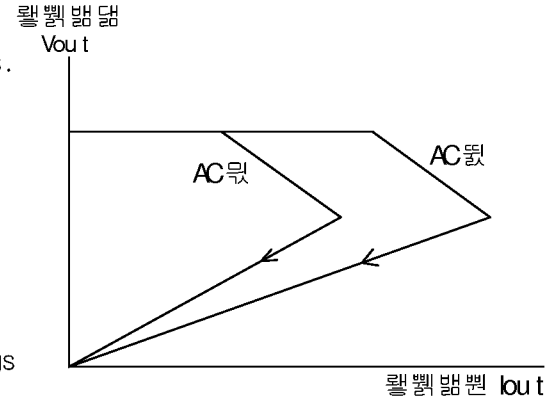


Figure 7

1.2.2 Overload Protection

Figure 8 shows the output characteristics of the secondary side when the over current protection circuit is activated by the overload on the output of the secondary side.
When the output voltage decreases during the overload, the auxiliary coil voltage of the primary also decreases. Then the VCC terminal voltage reaches the shutdown voltage and stops operation.
At this occurrence, VCC terminal voltage is increased by the charging current from the startup resistance Rs and becomes the intermittent operation of restarting on the circuital operation voltage.
If the transformer comprising a number of output windings is not combined adequately, intermittent operation might fail, with the auxiliary coil voltage on the primary side does not decrease even when the output voltage decreases.



?괰 밺뙶뢯뿱뛹븄됖벫맜

If the intermittent operation does not occur, the overload protection circuit can be engaged.
The output voltage on the secondary side decreases during the overload (i.e. when the drain current is limited by the over current protection).
The secondary error amplifier and the photocoupler are cut off by this occurrence. STR-W6700 Series engages the overload protection when the FB signals are not generated and the operation of the OCP continues as shown in Figure 9.
If the SS/OLP terminal voltage continues to increase and reaches the VSSOLP(OLP)(Typ5V), oscillation stops and the latch protection operation is engaged.

The time sequence that leads to the latch protection can be estimated based on the time that ISSOLP(OLP) was a rectifying current circuit.
C(Condenser capacity) x V(Condenser charging voltage 5V)=ISSOLP(OLP) x t(hours) equation(2)
Because ISSOLP(OLP) is dependent on the SS/OLP terminal voltage. If the SS/OLP terminal increases, ISSOLP(OLP) decreases. Yet, the equation (2) does not yield an accurate value.
Therefore, you need to take into full account the actual load conditions.
Check whether the latch protection operation is available even when the power supply startup engages the OCP protection.

1.2.3 Operations of Power OFF

During power OFF, the voltage of the external condenser across the SS/OLP terminal is discharged due to the reset circuit of the device. The reset circuit is not turned on during the power-down mode (i.e. when the constant voltage circuit of the device is activated).

1.2.4 Disabling the OLP Circuit

To disable the OLP protection operation by activating the Soft Start add a resistor of 47kΩ (approx.) to SS/OLP terminal. It disables the OLP operation on startup and overload condition.

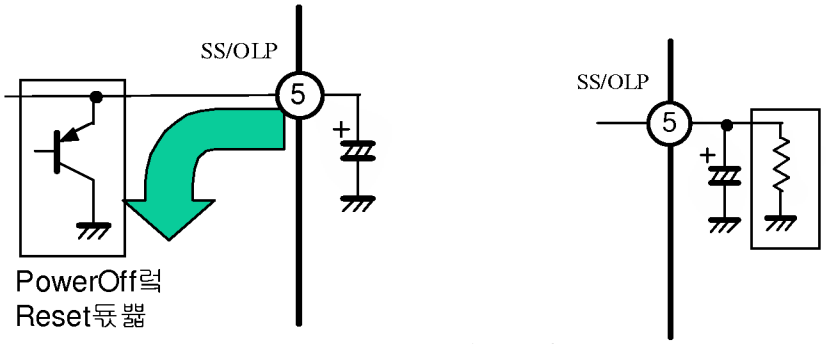


Figure 9

1.3 About the FB Terminal (Terminal No.6)

FB terminal operation can be divided into two:

- Normal Operation (Control over constant voltage circuit)
- Control over Standby mode

Refer to section 1.6 for information about the control during the St-By.

1.3.1 Constant Voltage Control Circuit

STR-W6700 adopts the current mode control circuit for the constant voltage control that provides excellent stability against medium load.

By comparing the voltage of the FB terminal and VOCPM of the inside of the IC, this device changes the peak value of the drain current (≒ 'ON' time) of MOSFET.

During the OFF, this device adopts a fixed oscillation frequency (about 22kHz) by engaging the quasi-resonance, which is reset signals from the transformer.

Figure 12 shows the timing chart, and Figure 13 shows the internal circuit diagram of the constant voltage control.

Figure 12 Constant Voltage Control (Disregarding Quasi-resonance signals)

Figure 13 Constant Voltage Control Circuit (Diagram)

The constant voltage control inputs the control signal (FB current) from the error amplifier on the secondary side into the terminal No. 6 by using the photocoupler.

The current and voltage of the input FB current is switched by the resistance of the inside of the IC (SW1 is set to ON usually), and the current becomes the feedback voltage VFB.

Voltage waveform (VOCPM) which is an reversed form of Drain waveform is implied to the FB comperator's input terminal.

This device adopts a current mode control circuit by controlling the peak value of the drain current with the FB Comparator. The FB current is reduced significantly or becomes zero during the overload as shown in Figure 12. Then, the overcurrent protection circuit limits the drain current to the preset current value. The FB current increases between the normal and extreme light load, as shown in Figure 12, and VFB starts to increase, reducing the drain current.
If VFB exceeds the threshold voltage (VFB(OFF),1.45 VTYP) of the FB terminal as in the case of extreme light load, the intermittent switching is engaged to prevent the output voltage on the secondary side from increasing.

1.4 OCP/BD Terminal (Terminal No.7)

The functions of the OCP/BD terminal can be divided into two parts:

- monitoring overcurrent(OCP)
- Control over Bottom Skip and quasi-resonance

Refer to section 1.5 for further control details of the Bottom Skip and the quasi-resonance operation.

1.4.1 Minus Monitoring of OCP Circuits

The over current protection (OCP) circuits of STR-X6700 Series is a pulse-by-pulse type OCP that samples the peak value of the MOSFET drain current and reverses oscillation output.
Design the over current monitoring resistance R5, R4 and C5 of external installation as shown in Figure 14. R4 and C5 is a filtering circuit used to prevent malfunctioning caused by the surge current that is generated by turning ON the MOSFET.
OCP operation that turns off the MOSFET when the OCP/BD terminal voltage reaches VOCPBD(LIM) by the overcurrent when the MOSFET turns ON and the switching current flows.

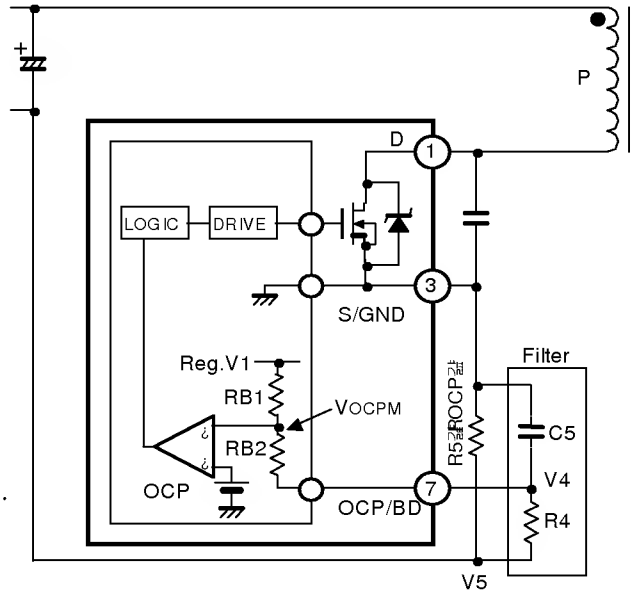


Figure 10

The threshold voltage COCPBD(LIM) of the OCP/BD terminal is 0/95V(Typ).
The OCP circuit adopts a minus monitoring circuit to impress the voltage between V1 and +R5 to the divided voltage by RB1, RB2, and R4, thereby generating the monitoring voltage VOCPM of the inside of the MIC.
Note that RB1 and RB2 are the IC internal resistance. Set the value of R4 at low ranges (100Ω □3330Ω) to reduce the effects of the margin of RB1 and RB2.

1.5 Quasi-resonance & Bottom Skip Quasi-resonance

1.5.1 Quasi-resonance Mode

Quasi-resonance matches the turn-on timing of the MOSFET to the bottom point of the voltage resonance waveform right after the transformer emits its energy, that is, a half cycle of the resonance frequency.

As shown in Figure 15, connect the voltage resonance condenser C4 between the drain sources, and connect the delay circuits C10, D3, D4 and R9 between the auxiliary coil D and the OCP/BD terminal(terminal No.7).

Quasi-resonance signals are generated when MOSFET is switched off and the auxiliary coil generates the Flayback voltage. Then, The BD Comparator inside the IC operates to enter the quasi-resonance mode.

Even when the transformer stops emitting energy, the quasi-resonance signals on the terminal 7 do not decrease due to the delay circuits.

It is due to the voltage drops below the threshold voltage VOCPBD(TH1)≒0.4 V after certain amount of time is passed from the discharging of the C10 by R4.

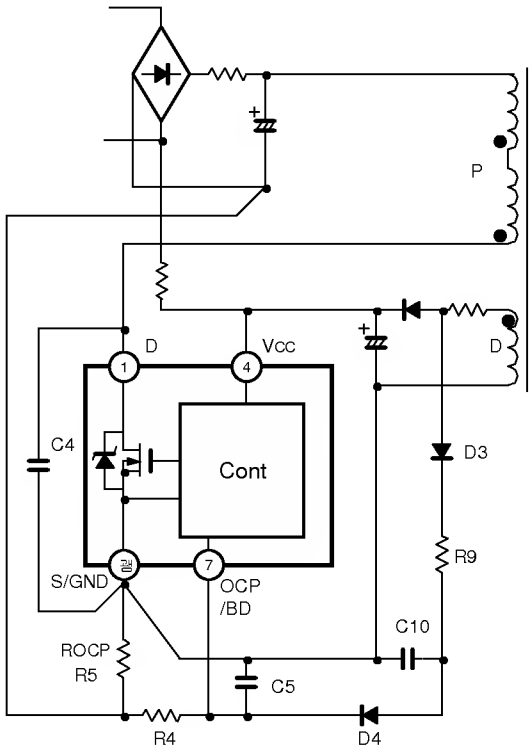


Figure 11

To adjust the delay time, adjust C10 while monitoring the operational waveform to have the Turn-on point of the MOSFET at the lowest VDS by monitoring waveforms.

STR-X6700 prevents the oscillation frequency from increasing under light to medium load, as well as it engages the quasi-resonance operation, and provides built-in Bottom skip function that prolongs the switching OFF according to the load. The switch timing between the quasi-resonance and the Bottom skip is described in the following section.

When the voltage of the quasi-resonance signals approved by the OCP/BD terminal is below VOCPBD(TH2)≒0.8 V, the PWM operation of the fixed frequency (≒22 kHz) begins by the internal oscillator. During startup or when the voltage of auxiliary coil is low due to its disconnection, the PWM operation begins and the oscillation frequency is lowered, and the stress on the internal MOSFET is reduced significantly.

The MOSFET remains turned off during the VOCPBD(TH1)≒0.4 V is implied after the quasi-resonance signal exceeds the VOCPBD(TH2)≒0.8 V.

This voltage difference between VOCPBD(TH1) and VOCPBD(TH2) prevents malfunctioning.

Additionally, take notice on setting up R9 and R4 that quasi-resonance signal to the OCP/BD terminal should be less than 5V where the voltage applied to OCP/BD terminal is 5V(MAX). Generally, 1.5V is adequate.

1.5.2 Bottom Skip Operation (Alternation between Quasi-resonance and Bottom Skip)

Basic operation of the Bottom Skip is switching between the quasi-resonance operation for medium loads and Bottom Skip operation for light loads according to the load on the secondary side by monitoring the Drain current (OCP/BD terminal voltage).

Current load status can be found by the OCP/BD terminal voltage when the Gate voltage dropping point of the IC internal MOSFET.

Also, MOSFET is turned on in compliance with previously described conditions by counting the occurrences of quasi-resonance signal's downfall (OCP/BD terminal voltage drops below the VOCPBD(TH1)) internally.

① From Quasi-resonance to Bottom Skip operation

During the quasi-resonance mode, the absolute value of VOCP is greater than VOCPBD(BS2).

From this point, the drain current decreases if the load is eased.

Therefore, base voltage is switched fully to the VOCPBD(BS1) automatically when the absolute value of VOCP becomes greater than VOCPBD(BS2).

Figure 16 shows the switching timing chart from the quasi-resonance mode to the Bottom skip mode.

② From Bottom Skip to Quasi-resonance

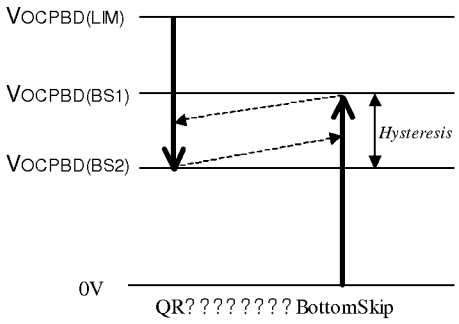


Figure 12

During the Bottom Skip mode, the absolute value of VOCP is smaller than VOCPBD(BS1). If the load becomes heavier, the drain current increases.

Therefore, base voltage is switched fully to the VOCPBD(BS2) automatically when the absolute value of VOCP becomes greater than VOCPBD(BS1).

VOCP is an OCP/BD terminal voltage when the MOSFET Gate inside the IC is cut off.

The standard voltages (VOCPBD(BS1), VOCPBD(BS2)) that engage the Bottom skip operation turn on the Histeresis operation automatically for stable operation.

1.6 Standby Operation

STR-W6700 Series provides the Burst Mode alternation function to reduce power consumption during the Standby.

Switches to burst mode automatically by providing adjustment switch to the secondary side and decreasing the output voltage from the standby modes such as waiting the remote control signal.

The adjustment switch on the secondary side reduces both the output voltage and the coil voltage of the transformer. Then, the voltage of auxiliary coil on the primary side is also lowered, cutting off the power supply to the IC VCC terminal (terminal 4) of the auxiliary coil. The VCC

terminal voltage is decreased due to power consumption of the IC itself.
When the voltage of the VCC terminal (terminal No. 4) of the IC reaches the power supply shutdown voltage (9.7V TYP), the IC stops operation and the current consumption of the IC goes back to the circuit current of the deactivated standby mode. The VCC terminal voltage (voltage of the terminal No. 4) begins to increase again when the startup resistance triggers charging of the backup condenser. IC starts operating again when the VCC terminal voltage reaches the operation voltage of the IC.
STR-W6700 switches automatically while reducing the difference between the Shutdown voltage and operation voltage to achieve increased operating frequency while avoiding increased loss at the startup resistor to cancel the magnetostrict noise of the transformer when switching from the Burst Mode. The switching is done by monitoring whether the FB terminal voltage exceeds the threshold voltage VFB(S) of the FB St-By. The range of the operation voltage of the VCC terminal is 1.45 V(TYP) during the St-By mode, and about one fifth of normal operation mode. Transient stage from the normal to Standby operation mode, oscillation of the IC is stopped by the Feedback current and the output voltage keeps decreasing. Check whether the output voltage of the secondary side meets the required voltage.
Transient stage from the Standby to normal operation mode, oscillation of the IC is stopped until the VCC voltage (terminal 4) reaches the threshold voltage 18.2V(TYP). Check whether the output voltage of the secondary side meets the required voltage.
The Standby operation is a Burst Mode caused by the intermittent operation of the IC. The output voltage decreases when the IC stops operation while the oscillation is stopped.
The Standby mode dramatically reduces the auxiliary coil voltage of the transformer that supplies power to the IC, triggering the intermittent operation that repeats switching oscillation by the startup resistance. Note that this device can only deal with Standby load during the Standby mode (during the intermittent operation).
Note that the transient to the normal load requires the power supply is fully switched to the normal mode before the transient where the interfering load application during the transient state may case startup errors.

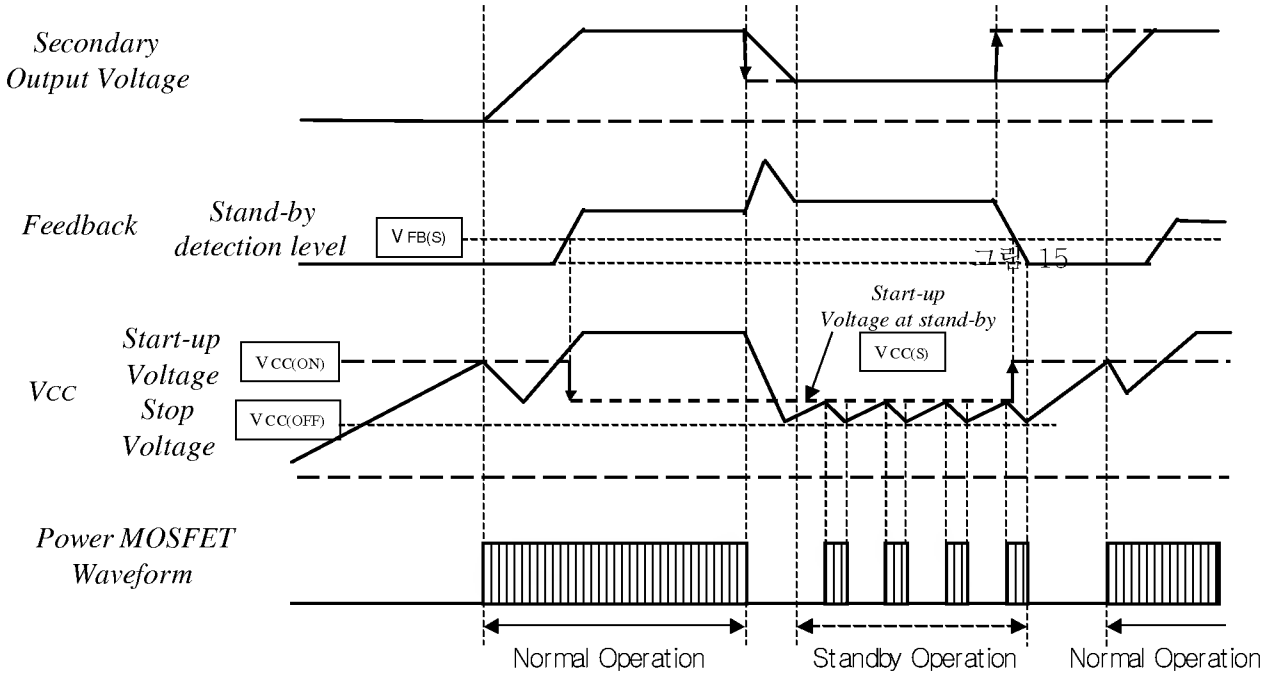


Figure 13

1.7 Step Drive Circuit

STR-W6700 Series adopts the Step Drive Circuit for the MOSFET driving as shown in Figure 19, so as to reduce noise during the turning ON. The RG1 limits the drive current to low current when turning on, and slowly increases the Gate voltage. And after about 0.9 μS, it increases the Gate voltage to RG1+RG2 rapidly. The drive voltage adopts a constant voltage drive circuit that maintains the VDRV=7.5Vtyp.
Therefore, it is not affected by the VCC voltage.
During the Turn Off, low resistance RG3 rapidly discharges the Gate charges of the MOSFET. The Drive Circuit of STR-W6700 is an optimal circuit that ensures enough gate voltage by changing the Gate voltage implied to the MOSFET in two stages to lower the Gate voltage and limiting the surge voltage when turning on.

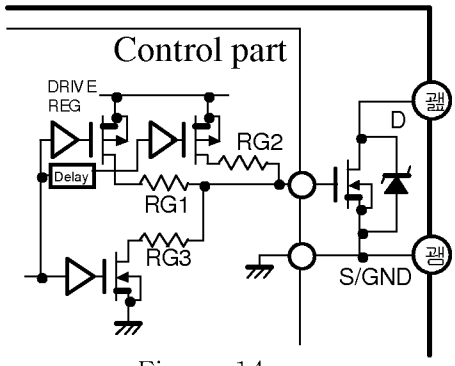


Figure 14

1.8 Maximum MOSFET ON time Limitation

MOSTFET ON time is limited for the transient states such as low input voltage and power on/off.
The maximum ON time is set at about 70% of the oscillation frequency (=1/fOSC, about 45μsec).
It is about 32μsec(Typ).
Check the lower ceiling of the input voltage at the power supply design.
Check the MOSFET ON time at the maximum load.

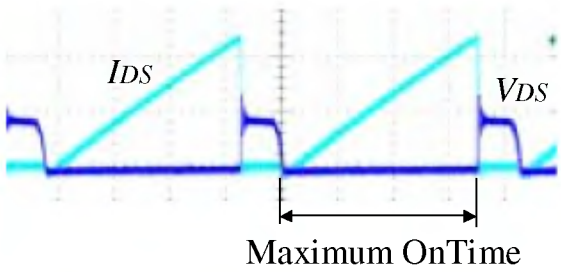
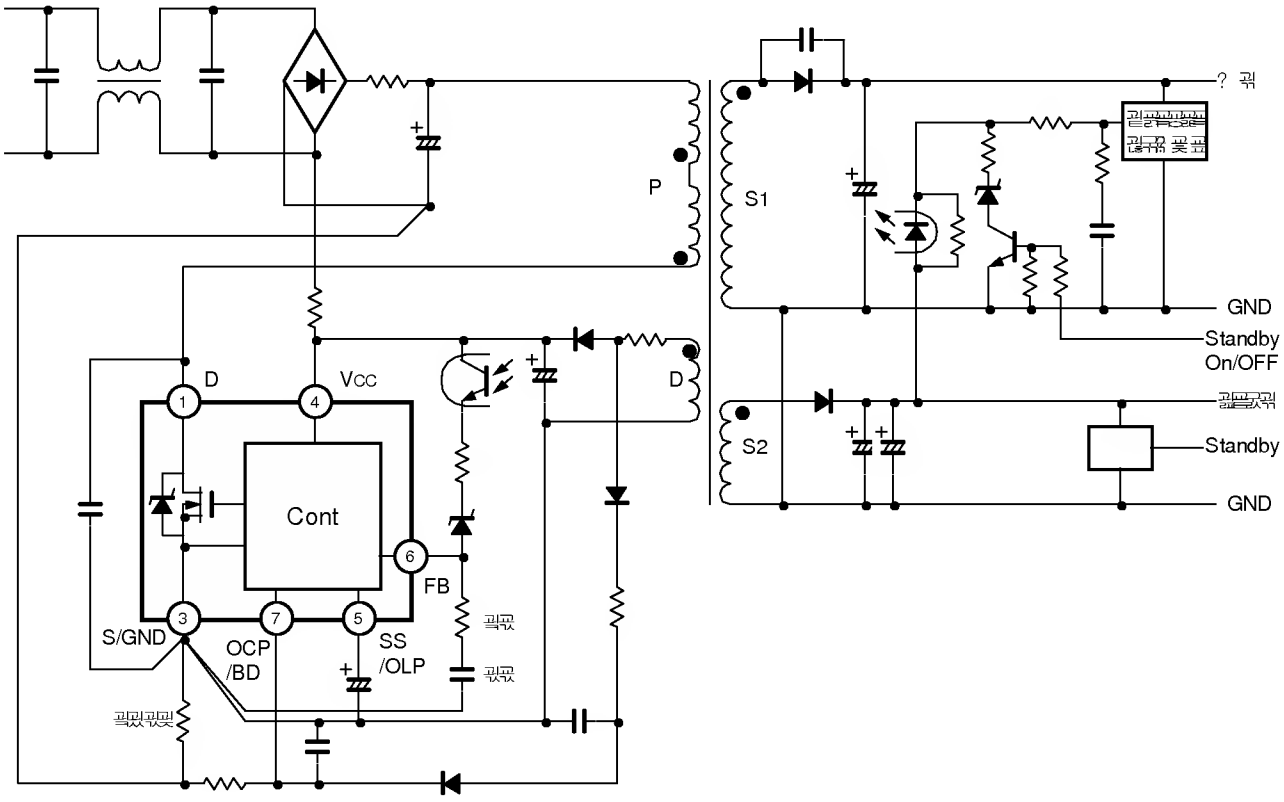
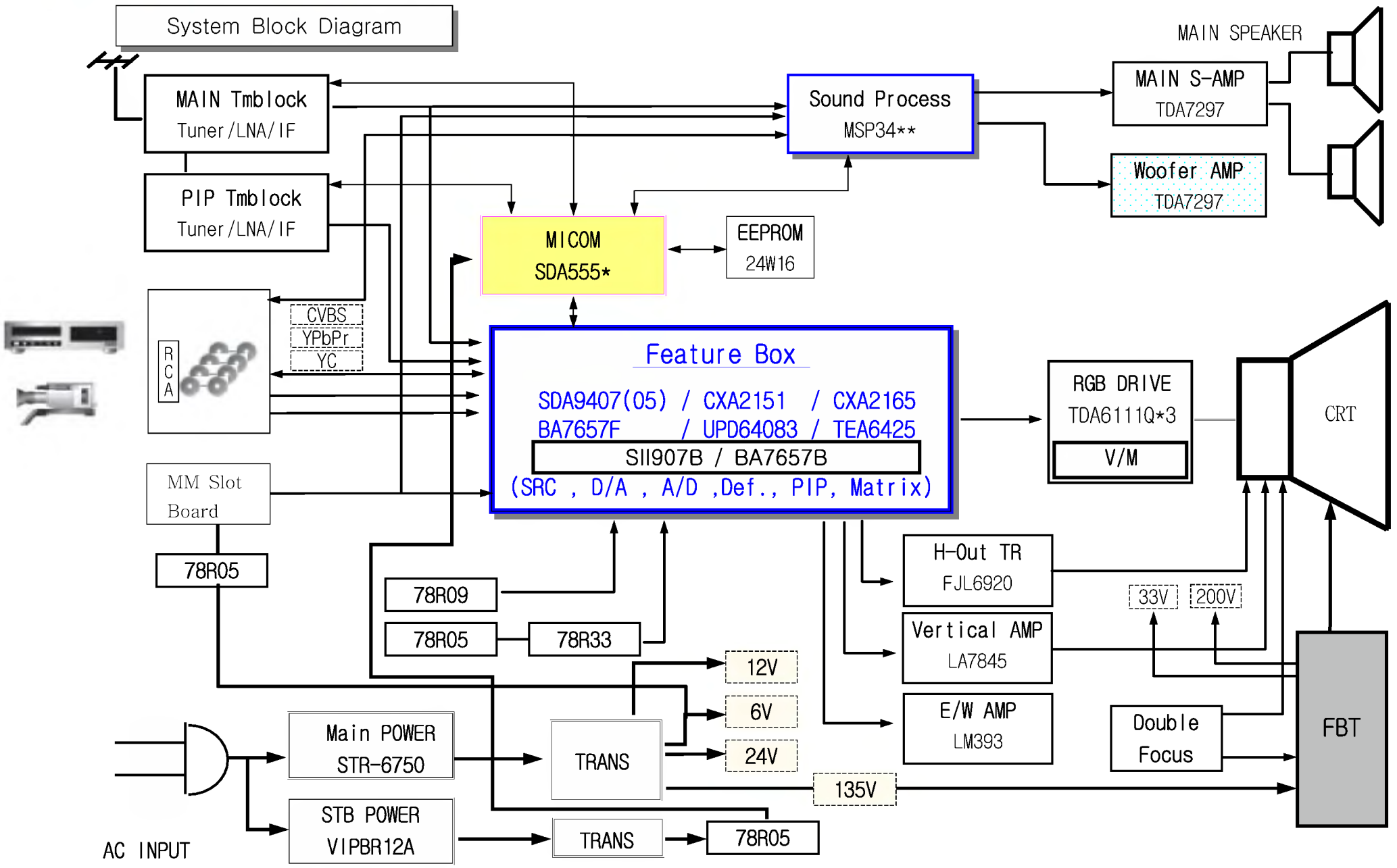


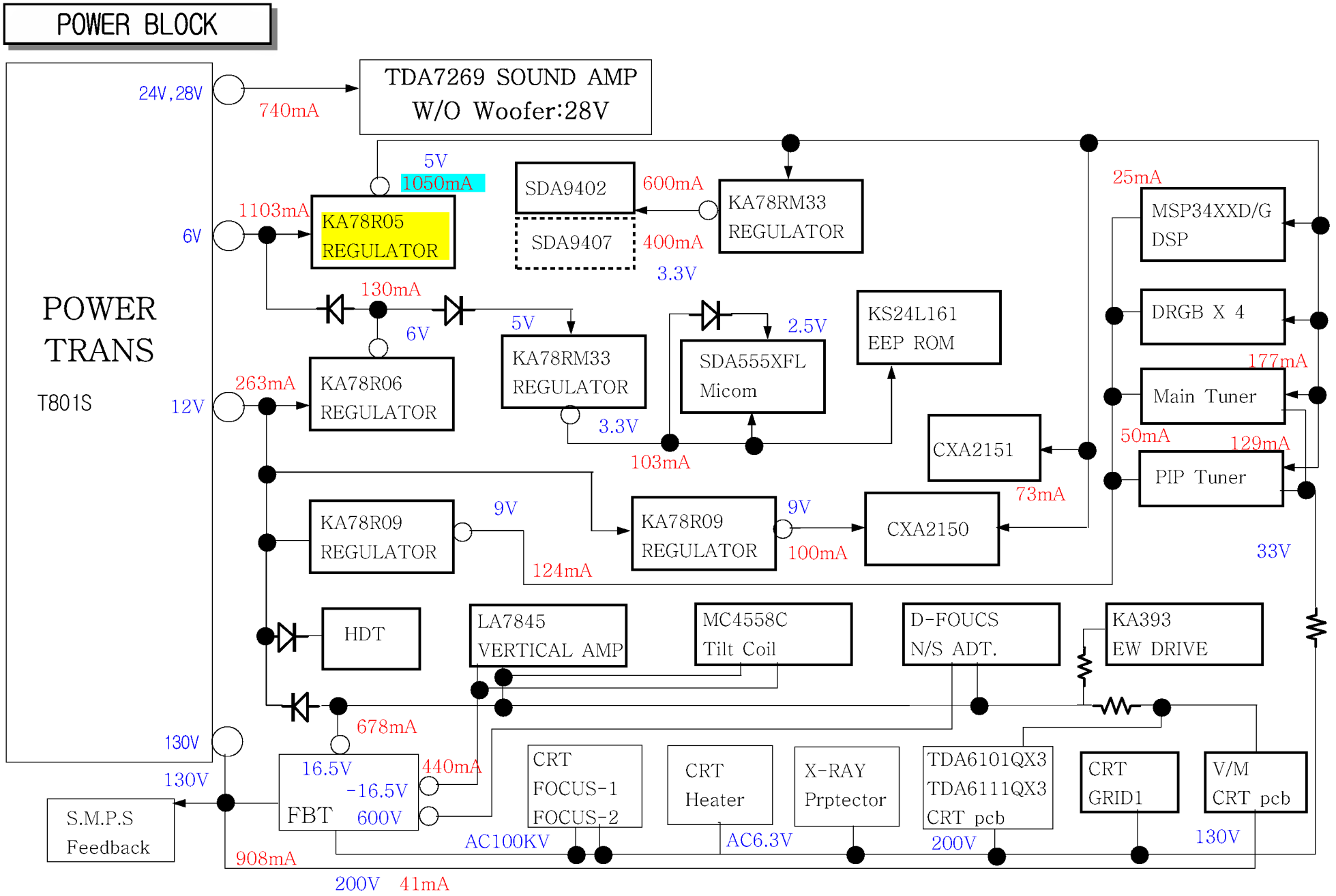
Figure 15

1.9 Application circuits



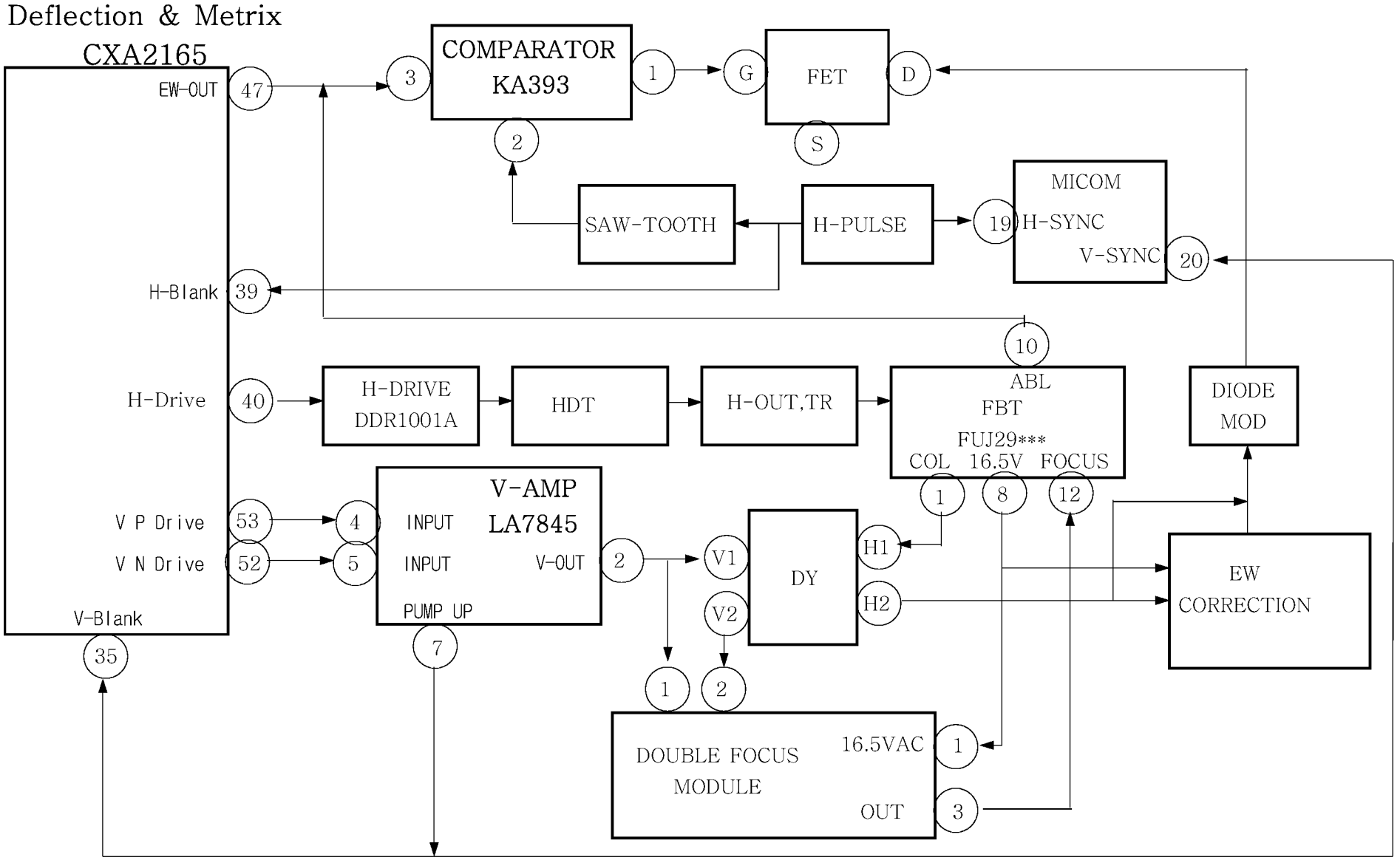
3. Block Diagram



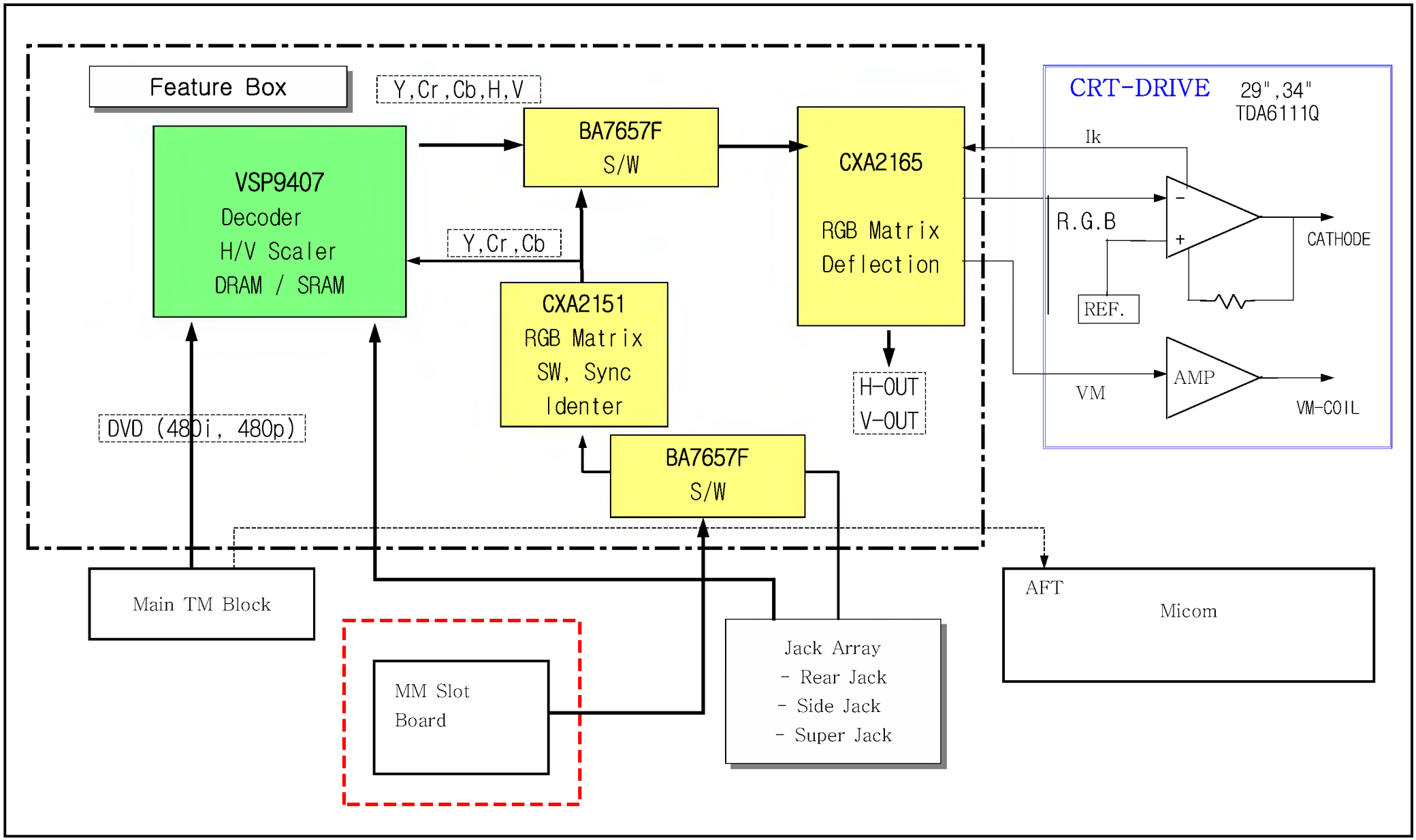

POWER BLOCK
POWER TRANS
T801S
24V,28V
740mA
TDA7269 SOUND AMP
W/O Woofer:28V
5V
1050mA
1103mA
6V
KA78R05 REGULATOR
SDA9402
SDA9407
600mA
400mA
KA78RM33 REGULATOR
3.3V
25mA
MSP34XXD/G DSP
DRGB X 4
130mA
6V
5V
KA78RM33 REGULATOR
3.3V
2.5V
SDA555XFL Micom
KS24L161 EEP ROM
177mA
Main Tuner
263mA
12V
KA78R06 REGULATOR
103mA
CXA2151
73mA
50mA
129mA
PIP Tuner
KA78R09 REGULATOR
9V
124mA
KA78R09 REGULATOR
9V
100mA
CXA2150
33V
HDT
LA7845 VERTICAL AMP
MC4558C Tilt Coil
D-FOUCS N/S ADT.
KA393 EW DRIVE
678mA
130V
130V
16.5V
-16.5V
FBT
600V
440mA
CRT FOCUS-1 FOCUS-2
CRT Heater
X-RAY Prptector
TDA6101QX3 TDA6111QX3 CRT pcb
CRT GRID1
V/M CRT pcb
S.M.P.S Feedback
AC100KV
AC6.3V
200V
130V
908mA
200V 41mA

Deflection BLOCK

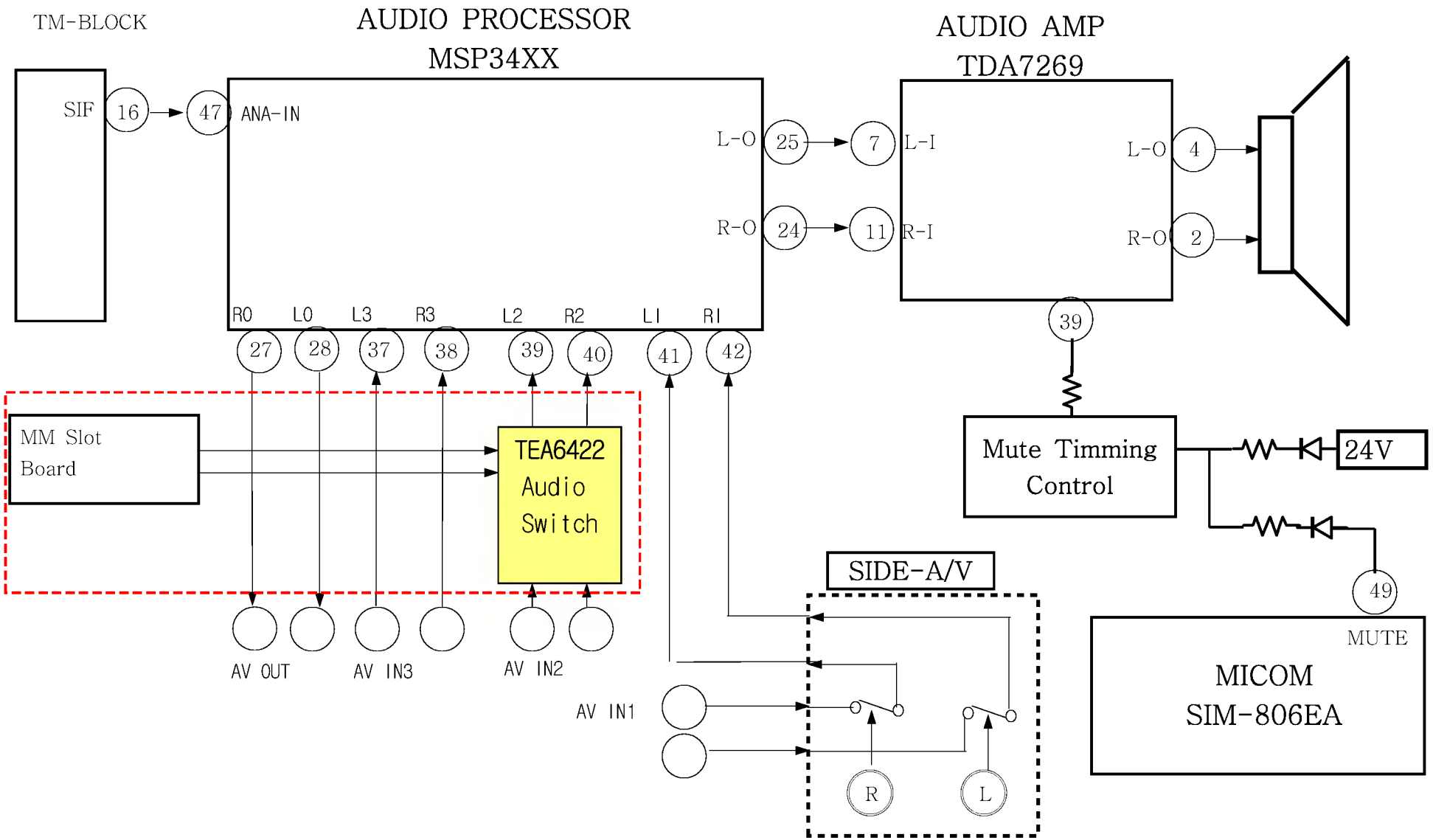
Deflection & Metrix



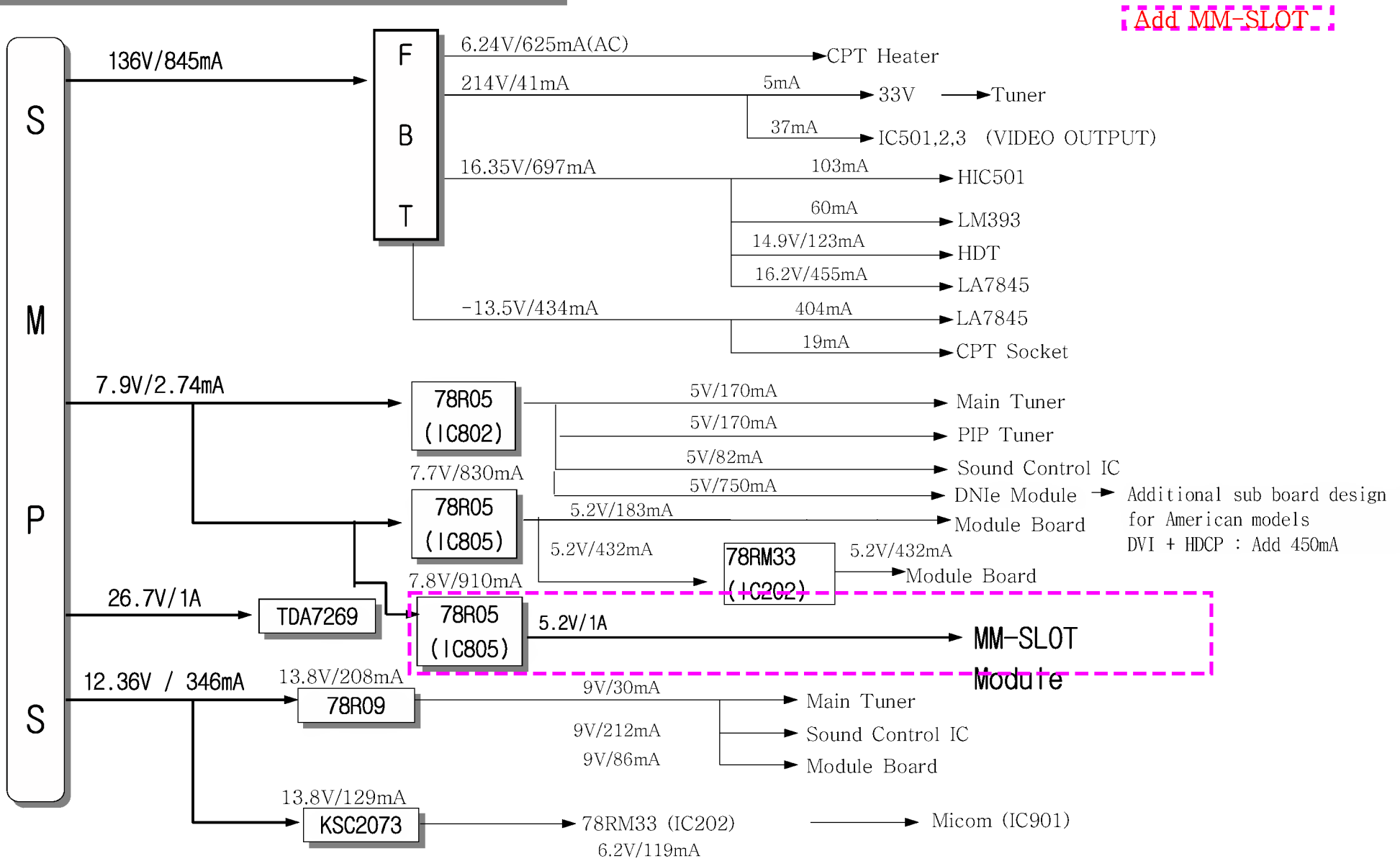
VIDEO SIGNAL BLOCK (KOREA)



SOUND SIGNAL BLOCK (KOREA)



5.2 Voltage/Current Analysis Diagram

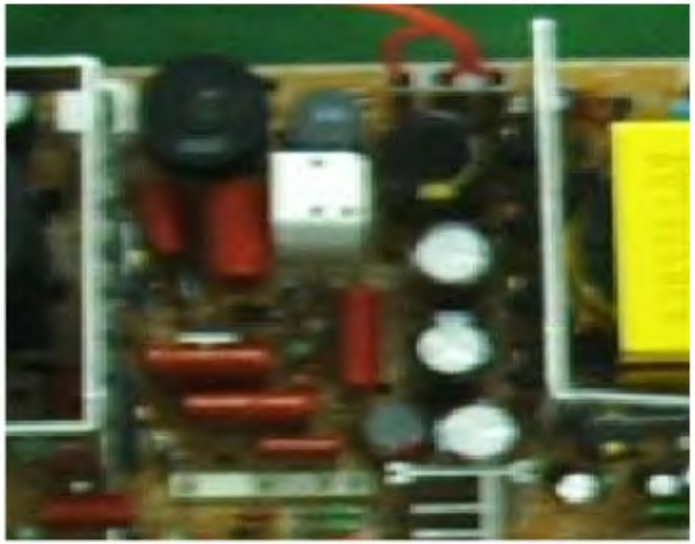
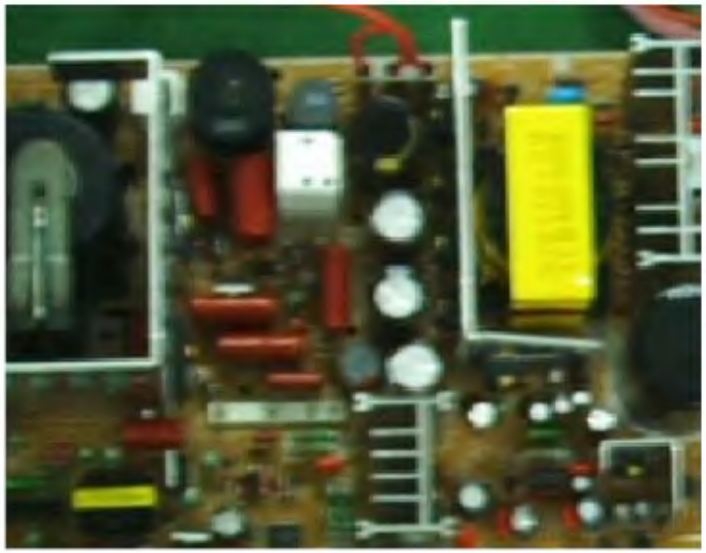
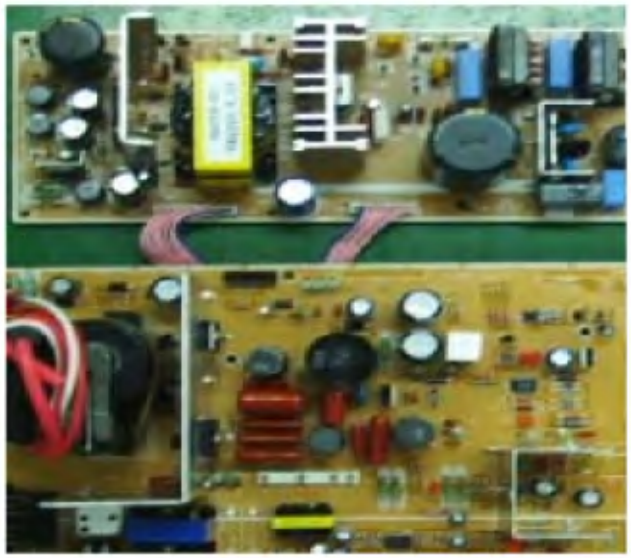


4. Considerations Related to SVC Property and Product Defects

Blue Note (Quality Failure Improvement Project)

Defect Classification	Detailed Defect	Defect Ratio	Major Improvement Countermeasure		Saving Objective
			Hercules Model Improvements	Hercules VE + Predator Additional Improvements	
Noise (630 Cases)	COIL Noise	0.83	◆ K55A tick noise - Cause: Short of Linearity and E/W coils - Counter Measure: Change Stick Type in the Bulk Type coil - Problem (oscillation sound (beep~) defect) - Separation of LR403S and LR405S. ◆ K55A tick noise - Cause: Short of Linearity and E/W coils - Counter Measure: Change Stick Type in the Bulk Type coil - Problem (oscillation sound (beep~) defect) - Separation of LR403S and LR405S. ◆ EPOXY coupling defect - Counter measure: Change FUH HV BOBBIN mold. ◆ Electric wire defect - Before change: Cut the wire with a nozzle by pushing. - After change: Pick a wire with a tongs and cut it off. ◆ No power due to FBT fault - Enhancement of HV FILM EMBOSS architecture (Line → Circular cone) - It has been applied to HV 7 system. - It has applied to HV 5, and HV 6 system. ◆ Duplication of Suppliers (Samsung Electro-Mechanics->PARTSNIC CO.,LTD.)	■ Removal of noise caused by the adjacent parts - When redesigning PCB, separate deflection parts (e.g. coils) by sufficient distance exceeding the human error distance. ■ Cause: It has been caused by not checking noise after a noise-related change. Counter measure: Check noise when a noise-related change has been made after development.	0.1
	PCB Noise	0.05			0.05
	DY Noise	0.02			0.02
	FBT Noise	0.01			0.01

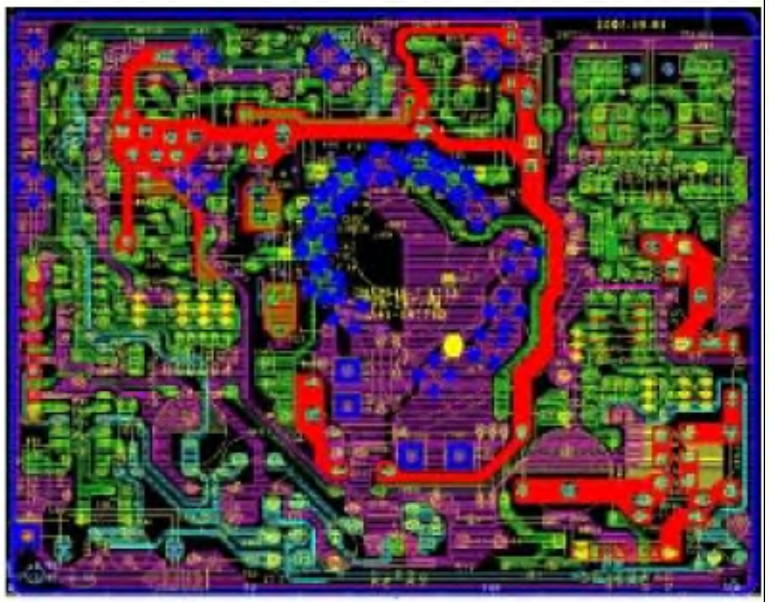
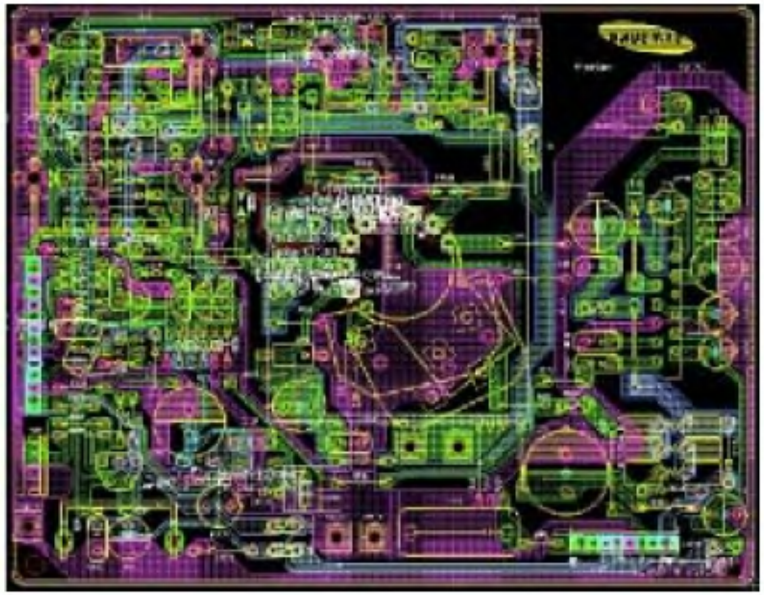
Reference: Considerations for quality improvement when changing main PCB

Considerations for quality	Hercules / Young Star	Hook/Predator
1. Noise and interference ■ **Cause: Deflection parts are closely located** **- Short circuiting of the parts due to human errors.** **- Interference between the parts due to adjacent coils.** ■ **Counter measure: Separation of the parts** **- Separate the parts so that a human error cannot short circuit them.** **- Separate coils** ★ **Noise and defects by interferences due to closely located parts will be removed.**		
2. Stress ■ **Cause: Closed located fuming parts** **- Deflection and power parts are closed located.** **(Heating parts such as horizontal, vertical and power are closely located)** ■ **Counter measure: Separation of parts** **- Secure required distance by separating power part from the main PCB** ★ **Existing PCB satisfies stress Since this measure lessens the stress on the heating part, the life time of the part would be extended.**		

Defect Classification	Detailed Defect	Defect Ratio	Major Improvement Countermeasure		Saving Objective
			Hercules Model Improvements	Hercules VE + Predator Additional Improvements	
PCB Replacement (303Cases)	No Power	0.20	◆ Horizontal TR J6920 defect - Counter measure: ESD problem: Reinforcement of the home of the horizontal TR Emitter port ◆ Transmitter defect Cause: loose contact caused by falling off the printed patterns on the spring and PCB Counter measure: SILK print on the PCB pattern to prevent loose contact.	■ Damage of CRT Drive IC - When redesigning CRT PCB, separate 220V power, output, screen, and the Drive IC with the maximum interval. ■ Cause: Intermittent discharge in SDI CRT Counter measure: Although the discharge of a CRT is not a defect, reduce the discharge by improving the process of SDI.	0.1
	Malfunction	0.03			0.02
	No Screen	0.03			0.02
	Color Defect	0.02			0.01
Adjustment (168Cases)	CG Adjustment	0.04	◆ Screen tilt - Counter measure: Development of Tilt coil (03.03.14) - Examination of operation and confidence: '03.3/25~26 - Separated application of TILT coil: 03.6/15 - Change of TILT circuit change from 5V to 3.3V	■ Cause: The difference of the shape of Degaussing and Tilt coil causes screen tilt, and color defect. Counter measure: Improve the shape forming of Degaussing and Tilt coil for all models.	0.03
	DY Adjustment	0.04			0.03
	FOCUS	0.02			0.02
Equipment (165Cases)	Equipment Scratch	0.08	◆ Scratch - Cause: It seems happen during distribution process. - Counter measure: Compensation of packaging considering the properties of design Counter measure establishment (applying protection CAP for vulnerable points)	■ Cause: The equipment seems to be scratched in installation step. Counter measure: A suggestion has been proposed to the design department so that the equipment can easily be moved, and fixed. ■ cause: Exterior scratch and stain by re-used package material during delivery. Counter measure: Guide the suppliers to package the product with a new sheet bag and then package the product with re-used packaging material.	0.04
	Gap between Parts	0.03			0.03
	Damage	0.03			0.03
	Noise	0.02			0.02

Defect Classification	Detailed Defect	Defect Ratio	Major Improvement Countermeasure		Saving Objective
			Hercules Model Improvements	Hercules VE + Predator Additional Improvements	
CRT (158Cases)	29"DF	0.08	◆ Smell: Smell reduced HOT-MELT has been applied (hot-melt: GP-3000 → GP-5000R) ◆ Color defect -Cause: Lower part D-COIL is formed upward when shape forming D- COIL and TILT COIL -Counter measure: Change of D-Coil, Tilt Coil shape forming. ('03.06.09 ~) ◆ CRT discharge => high-pressure leak output 2~4KV by internal Frit bubble. SOFT high-pressure process through DOWN.	■ Cause: Intermittent discharge in SDI CRT Counter measure: Although the discharge of a CRT is not a defect, reduce the discharge by improving the process of SDI. 훈민정음 SDI 방전 개선 안	0.04
	32"DF	0.07			0.04
	34'DF	0.02			0.01
TR	H-OUT TR	0.11	◆ Horizontal TR J6920 defect - Counter measure: ESD problem: Reinforcement of GND of horizontal TR Emitter port. J432 : Jumper---> F/B (6mm), L404 : Jumper---> F/B (6mm)	◆ Damage of horizontal TR Cause: The influx of surge and noise Counter measure: When designing CRT PCB and main PCB, separate major parts. Since the number of PCB is reduced, wire shape forming becomes simple so that the horizontal TR defect is expected to be reduced.	0.05
	TR	0.01			0.01

Reference: Considerations for quality improvement when changing CRT PCB

Considerations for quality	Hercules / Young Star	Hook/Predator
1. Damage by Discharge ■ **Cause: The influx of surge caused by discharge.** **- If CRT Drive IC is damaged, no screen would be displayed.** **- The influx from F/B signal port may destroy the H-TR.** ■ **Counter measure: Separate them by sufficient distance.** **- Separate CRT socket port, power and major signal ports by sufficient distance.** ★ **"No screen", and "No power' defects by damage of CRT Drive IC and H-TR are expected to decrease.**		

5. Considerations for Factory Data and SVC of SVC Mode

DEFLECTION	조정값
V Amp	조정
V Shift	조정
H EW	조정
H Shift	조정
V Linearity	조정
Upper Linearity	FIX
Lower Linearity	FIX
V SC	FIX
H Parabola	조정
Upper Corner	조정
Lower Corner	조정
H Trapezium	조정
Bow	조정
Angle	조정
V Position	FIX
CXA Left Blk	FIX
CXA Right Blk	FIX
MM-SLOT OffSet	조정값
V Amp	FIX
V Shift	FIX
H EW	FIX
H Shift	FIX
V Linearity	FIX
Upper Linearity	FIX
Lower Linearity	FIX
V SC	FIX
H Parabola	FIX
Upper Corner	FIX
Lower Corner	FIX
H Trapezium	FIX
Bow	FIX
Angle	FIX
V Position	FIX
CXA Left Blk	FIX
CXA Right Blk	FIX

480P OffSet	조정값
V Amp	FIX
V Shift	FIX
H EW	조정
H Shift	조정
V Linearity	FIX
Upper Linearity	FIX
Lower Linearity	FIX
V SC	FIX
H Parabola	FIX
Upper Corner	FIX
Lower Corner	FIX
H Trapezium	FIX
Bow	FIX
Angle	FIX
V Position	FIX
CXA Left Blk	FIX
CXA Right Blk	FIX
1080i OffSet	조정값
V Amp	조정
V Shift	조정
H EW	조정
H Shift	조정
V Linearity	조정
Upper Linearity	FIX
Lower Linearity	FIX
V SC	FIX
H Parabola	조정
Upper Corner	조정
Lower Corner	조정
H Trapezium	조정
Bow	조정
Angle	조정
V Position	FIX
CXA Left Blk	FIX
CXA Right Blk	FIX

VIDEO ADJUST 1	조정값
R CutOff	조정
G CutOff	FIX
B CutOff	조정
Color On/Off	FIX
CR OffSet	조정
CB OffSet	조정
R Drive	조정
G Drive	FIX
B Drive	조정
Sub Bright	조정
Sub Contrast	조정
Sub Color	FIX
Sub Tint	FIX
CTI Level	FIX
COL Axis	FIX
LTI Level	FIX
VSU	FIX
Melody Volume	FIX
LTI Mode	FIX
VIDEO ADJUST 1 Offset	조정값
Sub Bright 1080i	FIX
Sub Contrast 1080i	FIX

VIDEO ADJUST 2	조 정 값
ABL Mode	FIX
Gamma	FIX
DPIC Level	FIX
DC Trans	FIX
ABL TH	FIX
VM Level	FIX
VM Coring	FIX
VM f0	FIX
VM Limit	FIX
VM Delay	FIX
SHP CD	FIX
SHP f0	FIX
SHP f1 & P/O	FIX
AKB Time	FIX
YC Delay	FIX
PIP YC Delay	FIX
BandPass 9407	FIX
HighPass 9407	FIX
VIDEO ADJUST 3	조 정 값
Pilot Low	FIX
Pilot High	FIX
H Comp	FIX
V Comp	FIX
Pin Comp	FIX
AFC Comp	FIX
Sync Phase	FIX
NR Off Value	FIX
CR Offset 480i	FIX
CB Offset 480i	FIX
Sub Color 480i	FIX
Sub Tint 480i	FIX
CR Offset 480p	FIX
CB Offset 480p	FIX
Sub Color 480p	FIX
Sub Tint 480p	FIX
CR Offset 1080i	FIX
CB Offset 1080i	FIX
Sub Color 1080i	FIX
Sub Tint 1080i	FIX
Video Mute Time	FIX

VIDEO 1080i	조정값
1080i H Comp	FIX
1080i V Comp	FIX
1080i Pin Comp	FIX
1080i ABL TH	FIX
VIDEO ADJUST DNIe	조정값
AD9883 R Cutoff	FIX
AD9883 G Cutoff	FIX
AD9883 B Cutoff	FIX
VIDEO ADJUST DNIe	조정값
NR Scale Max	FIX
NR Scale Min	FIX
NR Sel	FIX
CE Cutoff	FIX
CE Upper	FIX
CE Alpha low	FIX
CE Alpha high	FIX
DCE Gain	FIX
CTI Gain	FIX
DEP TH Cor	FIX
DEP OV Gain	FIX
DEP R INT	FIX
CTE Gain	FIX
2150 system	FIX

적용모델	CT-29A20HR	CT-32A10HR
Option		
1. CRT	4:3	16:09
2. PIP(D/W)	On	On
3. 3D-COMB	Off	Off
4. Hi Deviation	Off	Off
5. Auto On	On	On
6. Virtual Sound	On	On
7. Woofer	Off	Off
8. AGC	Off	Off
9. Burst Screen	On	On
10. OthersCabinet	Others	Others
11. LNA Option	On	On
12. LNA Plus	On	On
13. NR Plus	On	On
14. DNIe Option	On/Demo	On/Demo
15. MM Option	On	Off

Development Model Types

☐ Chassis

Red parts: Changes compared with K55A

지역	28"	29"	32"	34"	36"
Z4		Non PIP, 4H-Comb, Direct Speaker 10WX2	Non PIP, 4H-Comb, Direct Speaker 10WX2	Non PIP, 4H-Comb, Direct Speaker 10WX2	단종
Z6		Non PIP, 4H-Comb, Mimi-Dome Speaker 10WX2	Non PIP, 4H-Comb, Mimi-Dome Speaker 10WX2	Non PIP, 4H-Comb, Mimi-Dome Speaker 10WX2	
Z7		Non PIP, 4H-Comb, Under Direct Speaker 10WX2 + 25W	Non PIP, 4H-Comb, Under Direct Speaker 10WX2 + 25W	Non PIP,4H-Comb, Under Direct Speaker 10WX2 + 25W	
A10		PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2	PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2	PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2	
M6		Non PIP, 4H-Comb, Mimi-Dome Speaker 10WX2			
A20	Non PIP, 4H-Comb, Semi-Dome Speaker 10WX2	Wise Link, PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2 ,	Wise Link, PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2 ,	Wise Link, PIP, 4H-Comb, DNIe, Mimi-Dome Speaker 10WX2 ,	

Changes compared with K55A

1) Chassis architecture: 1 Board → 1.5 Board
2) FBT: C-Block internal-type
3) Hybrid VM IC used
4) Tuner changed (Samsung Electro-Mechanics → ALPS)
5) UI changed
6) Sound output changed (15W→10W) & Speaker changed (from Semi dome to Mini Dome)
7) Stand-By Trans added (independent stand-by circuit adopted)
8) DVI circuit included in F/B
9) Deletion of 3D Comb in all models
10) CRT related change

Inch	28"	29"	32"	34"	36"
Changes by CRT	Introduction of new inches	Clear Type → Application of Semi-Tint Double Focus → Single Focus	Clear Type → Application of Semi-Tint Double Focus (With V)-> Double Focus (W/O V)	Introduction of SDI CRT (TSB cannot be used)	Dropped

6. MM SLOT related information

MM-SLOT Module Development Plan

Rival Company/Technology Trend

☐ **Trend of Rival Companies**

☞ **Popularized adoption of display support functions for digital storage media**

- **Sony** : Memory Stick (Flat 28"~36")
  (Media Playback, JPEC Still Image support)
- **Panasonic** : Secure Digital (Flat 24"~36")
  (JPEG Still Image, AAC Sound support)
- **Sharp** :Integrated PC card slots (LCD 13"~21")
  (Supports SD, MMC, SMC, CF, and MS)

☐ **Technology Trend**

- According to the increase of the capacity of memory card, supported functions include functions for video as well as function for still images.
- Support from single to multi cards

Product Concept

☐ Product Concept

☞ **Improvement of Functional Competitiveness through Multi-Memory Slot Support**

- Target: 29"/32"/34"
  Young Start Chassis applied A20 model

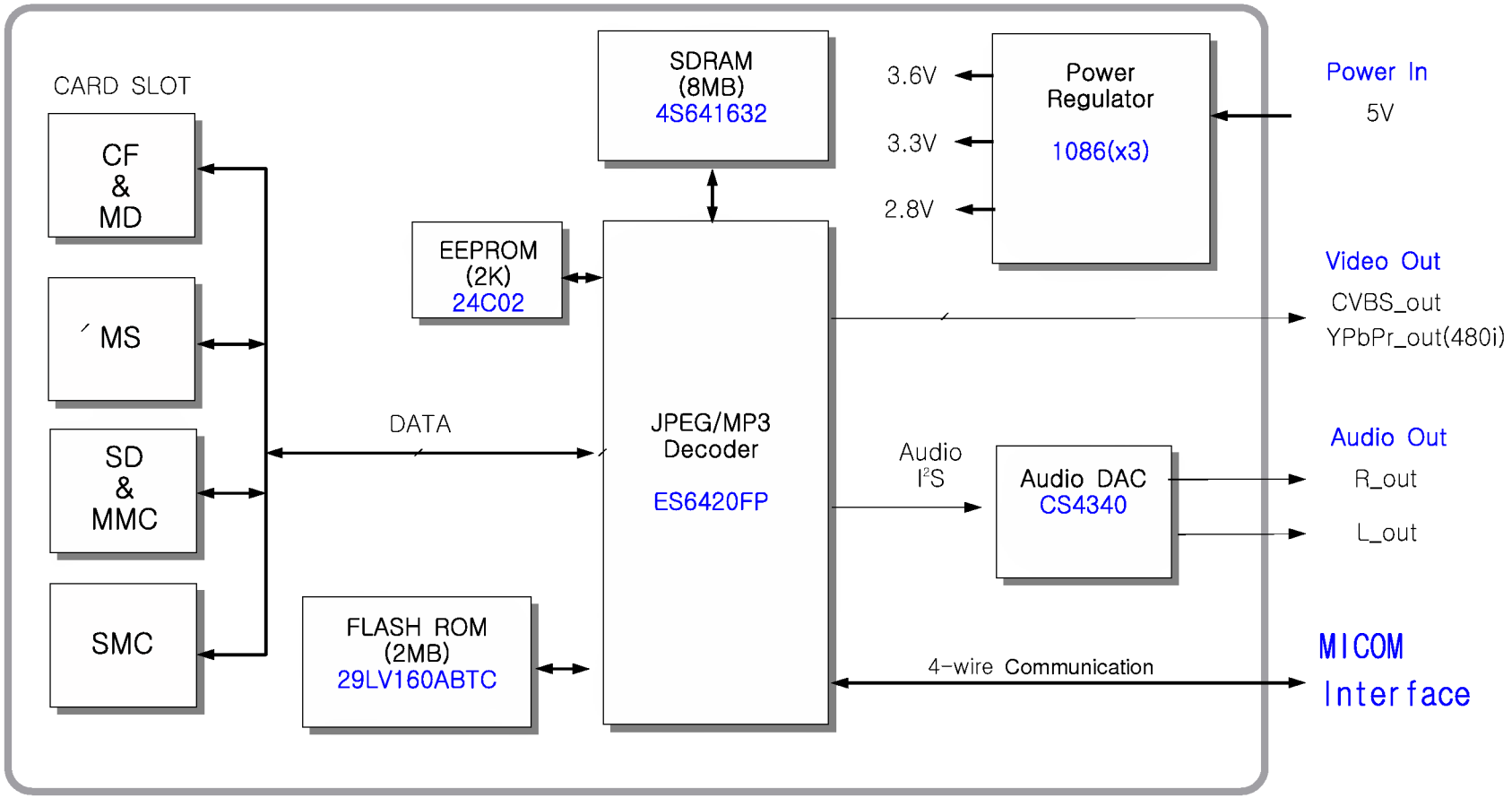
☐ **Differentiation**

- Multi memory card support
  .MS/CF/MMC/SD/SMC (5 types)
- Supported formats and functions
  .JPEG image playback
  .MP3 music file playback
  .Slide show
  .Background music function
- Application of easy user interface

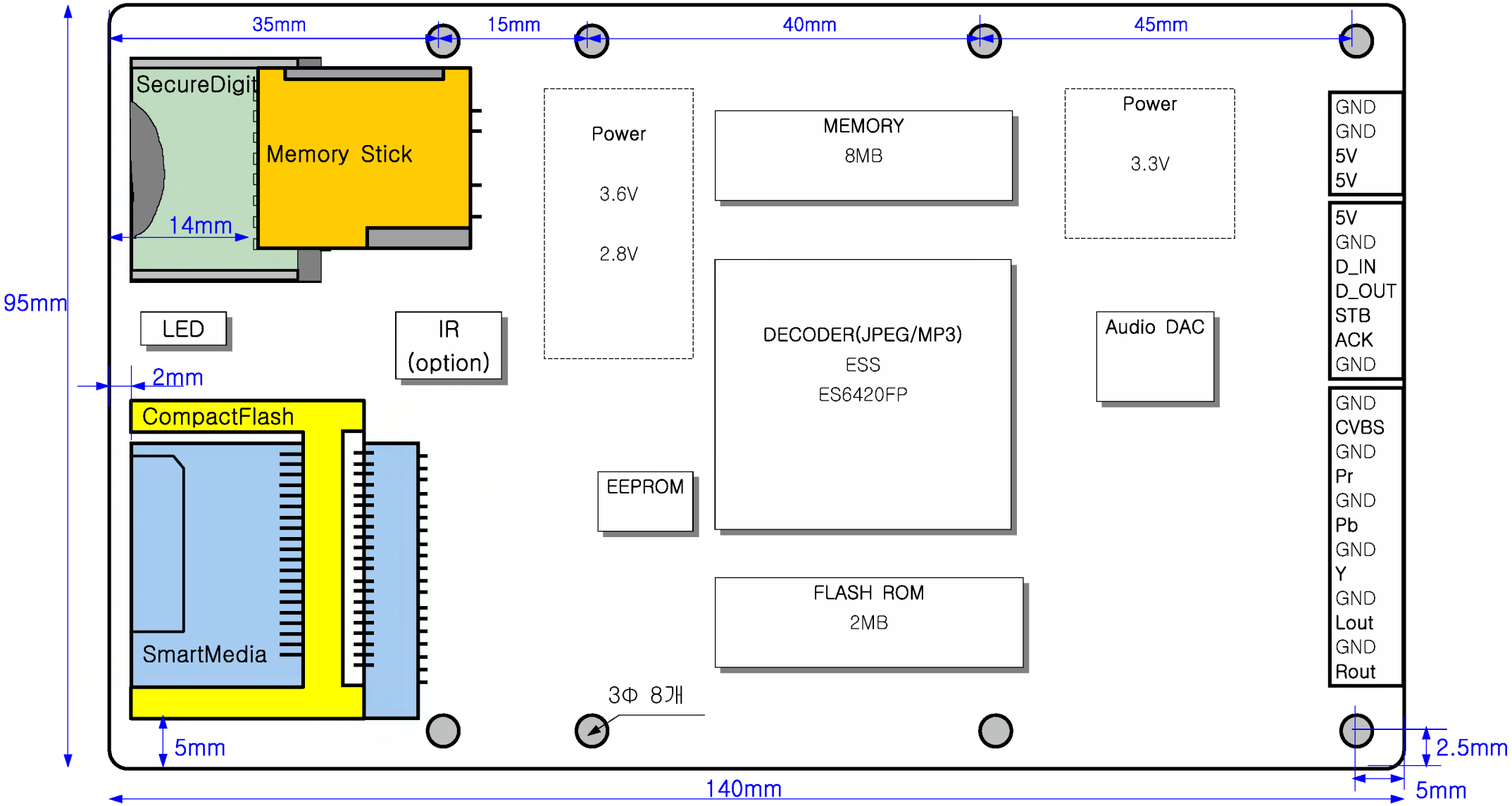
Major Function Specifications

NO	Item	Application	Description	Remarks
1	**Supported Memory Card Types**	Memory Stick Smart Media Card Multi Media Card Secure Digital Card Compact Flash	6 card types supported by the current module.	Except for xD Picture Card, and Memory Stick Pro..
2	**Supported Formats**	Photo: JPEG Music: MP3	Supported formats of memory cards that can be decoded and played.	Except for video formats
3	Read/Write	Read(Play) only	A function to play (read) saved data A function to save data in a memory card or to edit saved data does not exist	
4	**Video-Out Signal**	CVBS YPbPr	Analog video signal type decodes JPEG data saved in a memory card, and display data on a TV.	
5	Audio-**Out Signal**	Analog L/R	Analog audio signal decodes MP3 files saved in a memory card and play them on a TV.	
6	**Resolution**	480i	Resolution of video output signal of JPEG data	
7	TV color system	NTSC/PAL	Video output signal types by TV systems	
8	OSD Language	Worldwide support	OSD languages implemented by the module	Marketing Conference
9	**Added Functions**	Photo Zoom Photo Rotate Music Slide show Music Repeat	A function to zoom-in a JPEG image(2x,3x and 4x) A function to rotate a JPEG image clockwise. A function to display a JPEG image playing an MP3 file simultaneously. A function to repeat playing a MP3 file.	

Block diagram



PCB Layout


35mm
15mm
40mm
45mm
95mm
SecureDigit
Memory Stick
14mm
LED
IR
(option)
2mm
CompactFlash
SmartMedia
5mm
Power
3.6V
2.8V
MEMORY
8MB
Power
3.3V
DECODER(JPEG/MP3)
ESS
ES6420FP
Audio DAC
EEPROM
FLASH ROM
2MB
3Φ 8개
GND
GND
5V
5V
5V
GND
D_IN
D_OUT
STB
ACK
GND
GND
CVBS
GND
Pr
GND
Pb
GND
Y
GND
Lout
GND
Rout
2.5mm
5mm
140mm